The Charging Circuit Technique for Super-Capacitor Power Pack

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Abstract

What is there to especially deliberate about charging a Super-Capacitor (SC) Power-Pack? Is it 'a matter of fact' type charging of any other capacitors, that we do? Well when the capacity is in Farads instead of usually used micro-Farads, the charging technique requires care. An uncharged Farad capacitor when put across a voltage source or a power supply for conventional voltage mode charging provides a 'short circuit' for a longer time compared to when micro-Farad capacitor is charged. This long duration of short circuit will make the power supply to go into an 'over-current' shut-down mode, or may go into 'hiccup' mode. Similarly by overcharging of Farad capacitor may destroy the internal SC cells of power pack and thus affecting the life-cycle. Also in order to maximize the energy store in the SC bank or Power Pack, it is often best to stack several SC cells in series to realize high bank voltages. When charging a SC bank or Power-Pack, it is preferable to use a Constant Current/Constant Voltage (CCCV) charging method in order to limit the very-high currents that would otherwise flow due to low Equivalent Series Resistance (ESR) of the SC-if charging is via a constant voltage. We will discuss these issues in this short note.

Introduction

Super-capacitors (SCs), also known as ultra-capacitors and electric double layer capacitors (EDLC), are finding use in a variety of power management applications. In automotive applications such as start-stop systems with regenerative braking SCs can provide the energy needed to engage the starter to restart the combustion engine as well as store the kinetic energy recovered during the braking. SCs are advantageous because they can be charged and discharged significantly more times than traditional lead-acid batteries, and can also absorb more energy quickly without degrading their expected life times. These capabilities also make SCs attractive for industrial backup power supply systems, quick recharge cordless power tools and remote sensors where the frequent replacement of batteries is not practical. In this short note we discuss the challenges related to charging these SCs (i.e. large values in Farads capacitors), and how to evaluate and select the best configuration for back-up energy storage system.

About the Back-up energy storage system

There are several system configurations of using SC banks as Power-Packs and energy storage system. For starting the concepts, we will need to target their energy storage configuration and then decide at what voltage the energy we can store. Selection of the configuration depends on power and voltage requirements of the load and the energy and voltage capabilities of SC. The block diagram of Figure-1 shows a high efficiency solution where the load requires regulated voltages (3.3V, 5V, 12V etc). The main supply of 48V is supplying Switching Regulator-2 (SW2) in normal operation while simultaneously charging SC bank to 25V through Switching Regulator-1 (SW1). When the main supply is disconnected, the SC bank then supplies SW2 to maintain load operation without interruption.

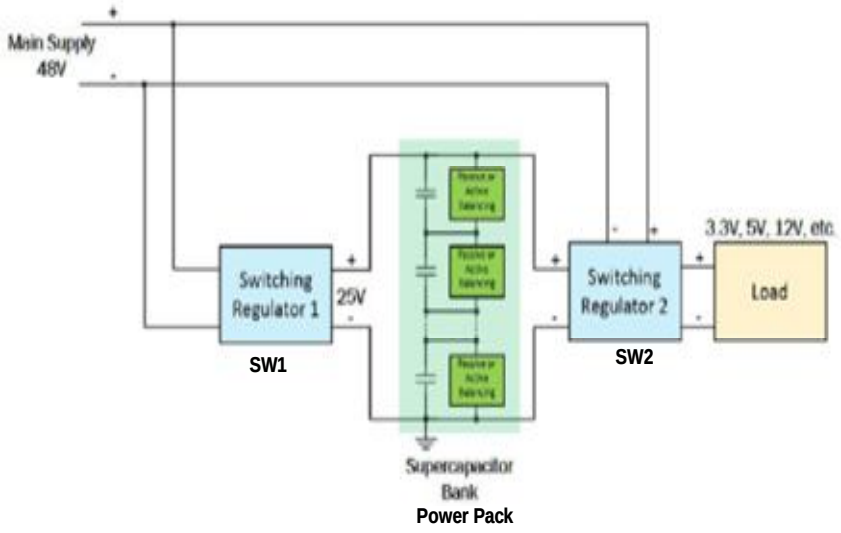

Figure-1: A Battery Backup System using a Super Capacitor Bank

The System Design Concerns & Challenges

Once we choose SC cell, the designer must select the target voltage at which each SC cell will be charged. This is done based on the rating curves of the SC. Most SC cells are rated in the range of 2.5V to 3V (2.75V nominally)-at room temperature. This rating of 2.75V falls at higher temperatures and with longer desired lifetime. Thus typically the target voltage should be set below the maximum rated voltage to extend the operating life of SC.

The next step is to get desired voltage for the bank of SCs and choosing SW2 topology. The SC bank or Power-Pack configurations can be in parallel, series or a combination of series strings in parallel. Since the cell voltage rating is typically under 3V and the loads often require higher voltages (in the case of Figure-1 it is 3.3V, 5V, 12V etc), the options for cell configuration and SW2 will be to use a single cell with boost converter or multiple cells in series and a buck or buck-boost converter regulator. To use a boost configuration, we must ensure that as SC

discharges, the voltage does not drop below minimum operating voltage of SW2. This value can be up to half of charged voltage of SCs and for this reason we will be illustrating a bank or Power-Pack comprising of series combination of SCs and a simple buck converter for SW1. Then if the energy requirements demand, multiple series strings chosen will be placed in parallel.

If a series combination of SCs is chosen, the number of cells used must be selected based on maximum desired voltage at the top of the string. More capacitors in series means higher voltage in SC string with less capacitance. For example consider choice of using two strings of four 10F/2.7V SC cells versus one string of eight in series of the same SC. The each SC cell can store energy of 36.45J and eight of them can store total 291.6J. Thus both these configurations store the energy of 291.6J. While the same total charge and energy can be stored in both cases (291.6J), the larger usable voltage range of the string makes the single series string i.e., charged up to $2.7\text{V}\times 8 = 21.6\,\text{V}$ advantageous, compared to 4 SC cells charged to $2.7\text{V}\times 4 = 10.8\,\text{V}$. Assume we have load requiring 5V bias; and the required minimum voltage for SW2 is 6V. With this assumption of SW2 electronics requirement, we can discharge the both the configurations up to 6V, and not below this level. Thus discharge voltage value of the strings in both the cases will be $\text{V}_{\text{discharge}} = 6\text{V}$. The charged voltages i.e. V_{charge} are 10.8V and 21.6V for the two cases as discussed.

The energy in SC is

$$\text{W} = \tfrac{1}{2}\text{CV}^2$$

and the energy that can be used is

$$\text{W} = \tfrac{1}{2}\text{C}\left(\text{V}_{\text{charge}}{}^2 - \text{V}_{\text{discharge}}{}^2\right)$$

For two strings of four series-capacitors the usable energy is

$$\text{W} = 2\times\left(\tfrac{1}{2}\left(\tfrac{10\text{F}}{4}\right)\left((2.7\text{V}\times 4)^2 - 6\text{V}^2\right)^2\right) = 201.6\text{J}$$

For one string of eight in series capacitors the usable energy is

$$W = 1 \times \left(\frac{1}{2} \left(\frac{10F}{8} \right) \left((2.7V \times 8)^2 - 6V^2 \right) \right) = 269.1J$$

Since both capacitor banks store the same total energy of 291.6J the string with lower voltage has greater percentage of charge/energy wasted i.e. unusable. In this case higher string voltage is preferable to fully utilize the SCs.

A third challenge is while considering how to charge SC bank or Power-Pack. Initially when the SC voltage is zero volts (completely uncharged state); the SW1 in Figure-1 has to work at a condition similar to an 'output short' for a fairly long period of time due to high capacitance of the order of Farads. A regular SW1 in Figure-1 i.e. conventional DC Power Supply (linear or SMPS) may get stuck in hiccup mode and fail to charge the SC bank. To protect the SC and SW1, addition current limit function is essential at the beginning of the charging state. A good solution would be for SW1 to provide continuous charging current for an extended time period at almost zero output voltage.

Charging Techniques for Super-Capacitor i.e. CCCV method

There are various methods to charge SC. Constant current/constant voltage (CCCV) is more commonly used and is preferred method as shown in Figure-2 (CCCV curve). At the beginning of the charge cycle the charging device SW1 of Figure-1 operates in a constant current mode providing a constant current to the SC such that its voltage is linearly increasing (rather almost linearly considering ideal capacity and neglecting fractional capacity). The SC is charged to a target voltage, at which time the constant voltage loop becomes active and accurately controls the SC charge level to be constant to avoid overcharging.

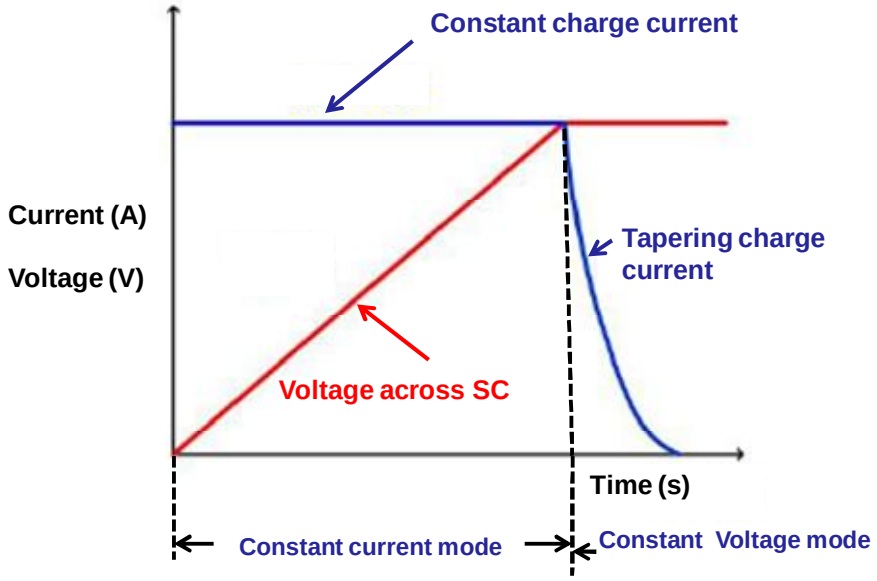

Figure-2: CCCV Super Capacitor Charging Control

Referring to Figure-1 as an example with main supply of 48V the SC bank voltage is 25V and load voltages of 3.3V, 5V, 12V etc., a synchronous buck converter for both SW1 and SW2 is appropriate. With the primary challenge relating to SC charging the choice for SW1 is critical. The ideal solution for SW1 would require power control functions that are capable of operating with input voltage of 48V and output 25V while also providing CCCV regulating capability.

Super-capacitor Charging Scheme

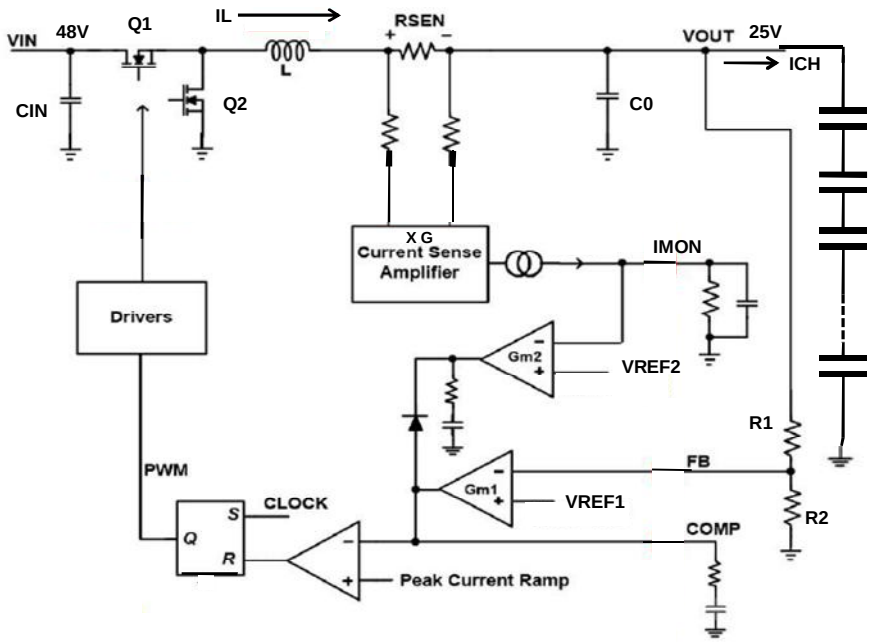

Figure-3: The CCCV Loop Block Diagram

The Figure-3 shows the block diagram of SC charging scheme-which is also called Synchronous Buck Converter. The usual buck converter has a diode in place of the grounded MOSFET switch Q2, and that diode conducts in the off-period of the main switch i.e. the series MOSFET (Q1). This fly-back diode is replaced by the grounded MOSFET (Q2) switch in order to reduce losses that take place in off-time due in the conduction of fly-back diode. Thus synchronous buck converter enhances the efficiency by reducing the fly-back losses, of conventional buck converter (i.e. with one series MOSFET switch and one fly-back diode driving inductor and load).

As shown there are two independent 'error amplifiers' named as Gm1 and Gm2. The Gm1 serves as constant voltage regulator and Gm2 serves as constant current regulator. We see that constant current regulator (Gm2) is feed-forward regulator and constant voltage regulator (Gm1) is feed-back regulator. The feedback voltage error amplifier Gm1 works for CV close loop feed-back control. This amplifier governs the PWM duty cycle only when VOUT reaches set value of

VSET (25V in our case of Figure-1 and Figure-2). First we see the classical feedback voltage loop working assuming that VOUT has reached the set i.e. 25V-that is SC bank is charged up to required VSET.

This Gm1 compares the feedback voltage at FB point to the internal reference voltage VREF1 and creates an output error voltage at COMP point. The FB point is connected to a resistor divider from the output voltage-i.e. SC banks upper point's potential; and is set such that FB point will be VREF1 when the output is at desired voltage call it VSET (in case of Figure-1 it is 25V). The COMP point voltage then represents the difference between the desired output voltage and the actual output voltage, i.e. representing voltage error signal.

This voltage error signal at COMP voltage is then compared to the 'peak current ramp'; an internally generated ramp signal from basic clock of say 600 KHz to control the switches for maintaining voltage output to a constant to VSET. The rising edge of the CLOCK (600 KHz) makes the SR Flip-Flop (FF) in SET state, i.e. Q of FF is HIGH, making the series MOSFET (Q1) in ON state and while Grounded MOSFET (Q2) is in OFF state. This makes VIN to charge the inductor and the IL is decided by LOAD resistance. This is ON time case. For case of very-very low ICH or load the current, as for open circuit case and VIN = VOUT, in this ON period.

When the internally generated RAMP reaches a value just greater than error voltage of COMP point, the output of this Ramp Comparator goes HIGH; causing RESET of the FF. This makes Q of FF LOW, thus switching OFF the series MOSFET (Q1) and switching ON the Grounded MOSFET (Q2), making the inductor current to fall linearly towards zero. This is fly-back or freewheel action conventionally done by a diode-but in this synchronous buck converter this Grounded MOSFET (Q2) is circulating the fly-back current-in the OFF period of Q1. This is OFF time case. For a case of very-very low ICH or load current, as for open circuit case, VOUT is 0V, in the OFF period.

In this voltage loop control we have output voltage regulated by Duty Cycle 'D' as follows

$$VOUT = D \times VIN \qquad D = \frac{t_{ON}}{t_{ON} + t_{OFF}}$$

The above voltage regulation via duty cycle is standard relation of a 'buck converter', where $VOUT < VIN$ as D is between zero and one.

This operation is simple voltage mode control of PWM. The load current will be almost zero $ICH \cong 0$, as the capacitor bank is charged to its set value VSET of VOUT of 25V as set. So the output voltage is maintained at VOUT set at 25V with almost zero current. Say if the capacitor bank is replaced by resistive load of RLOAD, then load current (ICH) would be given by inductor as ICH = VOUT/RLOAD at VOUT of 25V. Here the equation to have set output voltage (VOUT) is by choice of R1 and R2 i.e. the output voltage regulation is having following expression

$$\frac{VOUT \times R2}{R1 + R2} = VREF1$$

$$VOUT = VREF1\left(1 + \frac{R1}{R2}\right) = VSET$$

The output current (ICH) is sensed by resistor RSEN (Figure-3), which is charging current for SC bank in CC mode-via Current Sense Amplifier of gain 'G'. The equation governing the output current regulation is via Gm2 i.e. in feed-forward loop is

$$ICH \times RSEN \times G = VREF2$$

$$ICH = \frac{VREF2}{G \times RSEN} = ISET$$

At the start of charging state of SC banks, the voltage is zero, or we say FB point voltage is less than VREF1, making the output of Gm1 high, thus making the diode in the Figure-3 (between output of Gm1 and Gm2) to conduct. Thus Gm2 gets connected to the COMP point. The current sense differential amplifier with Gain 'G' senses the inductor current, which is a triangular ramp up and ramp down (cycle by cycle) and then converts to 'average charging current' as averaged on IMON point. This average charge current is compared with the VREF2 at Gm2.

This Gm2 is connected till IMON point voltage is greater than equal to VREF2. Thus at the start of the charging stage before the SC bank voltage reaches the target (in case of Figure-1 and Figure-2 it is 25V), the error amplifier Gm2 is dominating and driving the COMP point, causing

the PWM output to achieve CC control mode. This control is feed-forward control, controlling the inductor current. When the feed-back loop Gm1 dominates i.e. when the load voltage VOUT is just above 25V, the feed-forward loop control stops as Gm2 disengages, making the controlled ICH earlier set by feed-forward control as zero.

When SC bank voltage is charged to target (for our case 25V) the charging current gets reduced causing IMON point voltage to fall low and CC loop disengages (when IMON < VREF2) and CV loop naturally takes over to control the COMP point and thereby controlling the output voltage a constant. The Figure-4 gives details of these two modes CC and CV while SC power-pack is charged.

We note that current sense differential amplifier with input resistor RSEN has high common mode voltage (in case of our example it is 25V).

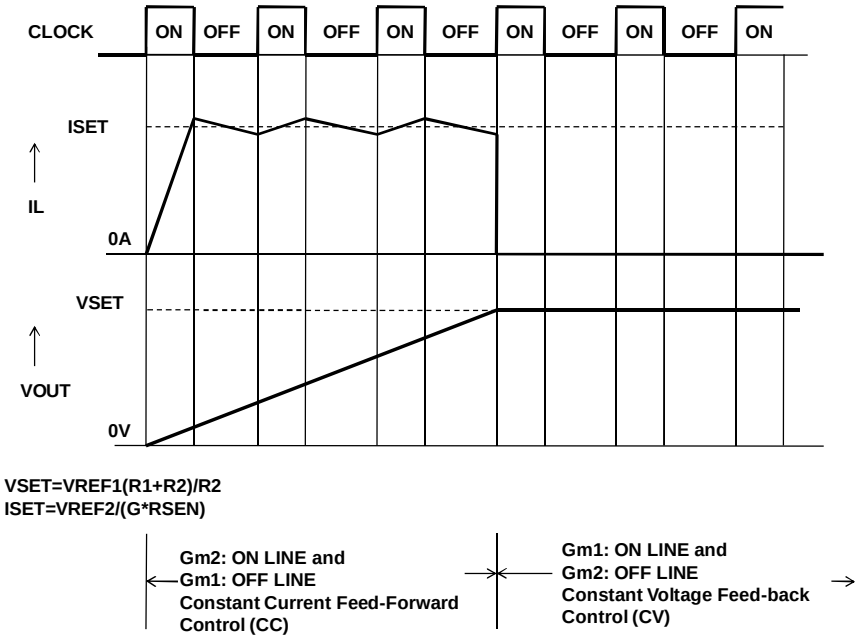

Figure-4: Switch mode control CC & CV mode

A high switching frequency (f_S) of 600 KHz allows using a small inductor and capacitor values. The inductor saturation current must be higher than the ISET or charging current ICH plus half the ripple current IRIPPLE, i.e. the usual rule for inductor selection in power convertor circuits

$$ISAT \geq ICH + \tfrac{1}{2} IRIPPLE$$

$$IRIPPLE = \frac{VIN \times D \times (1-D)}{f_S \times L}$$

The indictor ripple current depends on input voltage VIN, duty cycle D = VOUT/VIN switching frequency f_S and inductance L. The maximum inductor ripple current happens at D = 0.5. Usually inductor is designed in range of 20-40% maximum charging current.

For input decoupling capacitor is used and is placed to the drain point of Q1 and source of Q2. This input decoupling capacitor must have enough ripple current rating to absorb input switching ripple current. The worst case RMS ripple current is half of the charging current when duty cycle D is 50%, and is estimated as

$$ICIN = ICH\sqrt{D(1-D)}$$

Similarly output capacitor also must have enough ripple current rating to absorb output switching ripple current. The output capacitor RMS current ICOUT is estimated as

$$ICOUT = \frac{IRIPPLE}{2\sqrt{3}}$$

The output capacitor voltage ripple can be calculated as

$$\Delta VOUT = \frac{1}{8LCf_S^2}\left(VOUT - \frac{VOUT^2}{VIN}\right)$$

These are usual selection formulas for use in circuit of power converters. The rules for selection of suitable MOSFETS also remain the same as for DC-DC (synchronous) buck converter circuits.

Conclusion

Super-capacitors (SC) also known as ultra-capacitors and electric double layer capacitors are finding use in variety of power management applications and are adopted as energy storage solutions like in certain automotive and consumer products due their intrinsic physical characteristics that provide advantages over traditional batteries. To maximize the energy store in the SC bank, it is often best to stack several SC cells in series to realize high bank voltages. When charging a SC bank, it is preferable to use a Constant Current/Constant Voltage (CCCV) charging method in order to limit the very-high currents that would otherwise flow due to low Equivalent Series Resistance (ESR) of the SC-if charging is via a constant voltage. The constant current makes charging losses controllable within SC, which can reduce heat generation and extend the life of SC.

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