Review of Fly-back Switched Mode Power Convertor Circuits for driving LED lamps with Power Factor Correction and Line Current Harmonic Reduction

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Abstract

Why put efforts to have improvements on a seemingly simple electronics to drive Light Emitting Diodes (LED) lamps? Well conventionally we place a full wave rectifier at AC mains can divide the rectifier output voltage by resistor-capacitor divider and then power LED lamps. Well doing so, we get the lamp driven, but at a cost of distorting the input AC line current. Not only this gives high distortion in current-but also we get a leading Power Factor much away from unity, of the order 0.2. Also this simple scheme is adding to the cost of electricity. Nowadays since the improvements in process and technology, the luminous efficiency of Light Emitting Diodes (LEDs) is significantly enhanced, as compared to other lighting sources e.g. high intensity discharge lamps, florescent lamps (FLs) and cold cathode FLs (CCFLs), LED has considerable advantages on mercury-free devices, low DC voltage driving, and ultra long life time (above 50 thousand hours). Due to the international petroleum crisis and green house effect, the whole world looks forward to the more efficient luminaries, and thus conventional lighting sources are progressively replaced by LEDs. At a time when lean manufacturing has become the mantra of industry, minimizing energy costs has assumed ever greater importance. It's not just a matter of controlling consumption, however, but of how that consumption is billed by the utility. This is where power factor plays a key role. Power factor is the ratio of real power to apparent power in an electrical system. The lower is the power factor; the higher is the current draw. Higher current requires thicker wires and a more robust infrastructure in order to minimize power dissipation. Because this increases cost to utilities, facilities with low power factors get charged at a higher rate. Fortunately, techniques exist to correct power factor and harmonics. In general the driver circuit design dominates the energy efficiency as significantly as the light sources. In other words the lighting product efficiency can be considerably improved via appropriate driver circuit. Moreover acquiring electrical energy from wall plug (AC line) is familiar way. However LEDs are more suitable to be driven by a DC voltage in accordance to their characteristics and thus efficient AC-DC conversion stage is necessary. In this note we will review and understand this concept-by recalling the concept of switched power converters (SMPS) especially fly-back converters; and then develop the concept of utilizing these circuits for this seemingly simple application of LED lighting. We will discuss various topologies of converter circuits to do this application-and then discuss the simplest one for practical application. This note will not discuss inductor design and winding techniques, and also not be dealing with duty cycle modulation by output voltage/current feed back-for output load regulation. This note will concentrate on the basics of fly-back switching modes for power conversion purposes-in view to enhance the input power factor and reduce the input line current distortion; and we will point out the most modern topology of the converter circuit and its efficient switching. Thus at the end we will see LED lamp driving is far more involved electronics than one may think.

Keywords: Fly-Back Converter, Continuous Conduction Mode, Discontinuous Conduction Mode, Quasi Resonant Valley Switching, Transformer Isolated Converters, Power Factor Correction, Single Stage Power Converter, Snubber, Volt-second area rule, Geometric Mean of ripple current

Introduction

Typically a lighting system with LEDs commonly uses a full bridge rectifier and a high frequency inverter with an isolated transformer that converts the switching converter output characteristics from a voltage source to a current source, thus ensuring stable driving LED fixtures. Since the Bridge Rectifier absorbs energy from the AC power line; only when the input voltage is higher than the DC link voltage, the input line current contains high harmonics which pollute the power systems and generates interference noise to disturb other equipments. The power factor (PF) is typically less than 0.6 and the Total Harmonic Distortion (THD) can be high and greater than 100%. In order to improve the consumption of the electrical energy and meet the power quality standards IEC 61000-3-2, the LED fixtures must incorporate power factor correction (PFC) circuitry. Usually PFC Circuits present better results related to PF and THD in the input current. Then AC power line can be utilized more effectively.

Basically these techniques can be realized in two forms, a) Two-Stage Configuration and b) Single stage configuration. In a two-stage topology an AC/DC converter with PFC is connected to the AC power line, followed by DC-DC converter. These two power stages can be controlled separately, and thus it makes both converters possible to be optimized. Other advantage of this two-stage topology is that bulk-capacitor of the PFC circuitry is located at the high-voltage side, resulting in more energy stored in the capacitor and hence a longer hold up time. We have used this two-stage approach in ECPS circuits.

The single-stage topology combines the PFC circuit and power conversion circuit in one stage. Due to this simplified power stage and control circuit in a certain way that allows the PFC circuit and power conversion circuit to share the same power switch. In spite of the single-stage approach, still conventional two stage power electronics dominates the commercial market for AC/DC power adapter in LED lighting system. The two stage approach employs two-stages: the first stage is using the non-isolated boost converter to perform input-current shaping and universal input voltage handling and the second stage is using an isolated fly-back converter to subsequently step down the boosted voltage to desirable load-regulated output voltage. Although the two-stage solution has drawbacks of high component count and cost and large size, it is still commonly used due to relatively simple and viable operation in wide power range and universal range applications.

A string of LED in series and/or parallel needs proper voltage and current to drive. A more efficient method of providing voltage level and electrical isolation between input AC power line and output driver circuit of the LED fixture is to adopt a high frequency isolated transformer. A number of isolated switched mode converters which is fundamentally classified into three types of a) fly-back converter b) forward converter and c) push-pull converters are developed in use of both LED driver and PFC circuit.

Comparing the three different isolated DC/DC converter topologies, it appears that the fly back converter converter is the best for this application because of several merits. In addition, for a single phase lighting applications, the fly-back converter is generally recommended as high power factor (HPF) input rectifying stage, especially for low

power levels (as in application for multiple LED), due to its simple circuitry and typical input characteristics. Therefore a two stage approach i.e. PFC stage followed by a LED driver stage is utilized. The two stage approach has good performance such as a near unity power factor and wide range of line input voltage variation. Besides the design procedure is relatively easy.

The main problem of the two stage approach is that the component counts are more. Several single-stage PFC LED driver circuit aimed at reducing cost, have been proposed previously. In the single stage approach the PFC stage is combined with the LED driver stage into a single stage; thus one or more power switches and corresponding controller is saved. Although both boost and fly-back converters are capable for single stage PFC applications, the boost converter finds more usage than the fly-back converter, partly because the existing control methods make it easier to control the average inductor current.

For low power applications the fly back converter is more attractive than the boost converter because of its simplicity. It provides the entire operation by use of single switch. Besides this input line voltage is not necessarily lower than the output voltage (which is essential for boost converter). Then a high power factor can be achieved by deliberately operating the converter in the Discontinuous Conduction Mode (DCM)-with a constant frequency. As a consequence the fly-back converter provides simultaneously a unity power factor to the utility line and appropriate output voltage to the LED strings as well as gives low component count (enhancing reliability, efficiency reducing cost), compared to conventional two-stage topology. We shall see various topologies of fly-back converter circuits and then study the techniques to enhance the power factor and reduce the harmonics.

The Fly-Back Converter-Basics Recall

Fly-back converter is the most commonly used circuit for low output power applications like LED Lighting. The output power of the fly-back switched mode power supply (SMPS) circuit may vary from few watts to less than 100W. The overall circuit topology of this converter is considerably simpler than other SMPS circuits. Input to the circuit is generally unregulated DC voltage obtained by rectifying the utility AC Voltage followed by a simple capacitor filter. In respect to energy efficiency fly-back circuits are inferior to other SMPS circuits-but its simplicity makes it popular in low power range applications. The commonly used fly-back is single switch system; however a two-stage topology exists that gives higher efficiency and is used for higher power output.

We draw the classical circuit as shown in Figure-1 (excluding the snubber part), as may be seen from circuit when the MOSFET switch is ON the primary side of the winding of transformer gets connected to the input supply with its dotted end to the positive side. At this time the diode D connected in series with secondary winding gets reversed biased due to induced voltage in the secondary (dotted end voltage being higher). Thus with the turning ON of the MOSFET switch S , the primary winding is able to carry current but the current in the secondary winding is blocked due to reverse bias diode. The flux

established in the transformer core and linking the windings is entirely due to the primary winding current. This mode of circuit we call as Mode-I of circuit operation. Figure-2a shows Mode-I operation (in bold line) the current carrying part of the circuit and the equivalent circuit shown in the Figure-2b. Under Mode-I the input supply voltage appears across the primary winding inductance and the primary current rises linearly. The following expression is a current rise expression

$$E_{dc} = L_{pri}\frac{\mathrm{d}i_{pri}}{\mathrm{d}t} \qquad i_{pri}(t) = \frac{E_{dc}}{L_{pri}}t + I_0 \tag{1}$$

Where E_{dc} is the input DC voltage, L_{pri} is inductance of the primary winding and i_{pri} is the instantaneous current through primary winding and I_0 is initial value of primary current at the instance when switch S is turned ON.

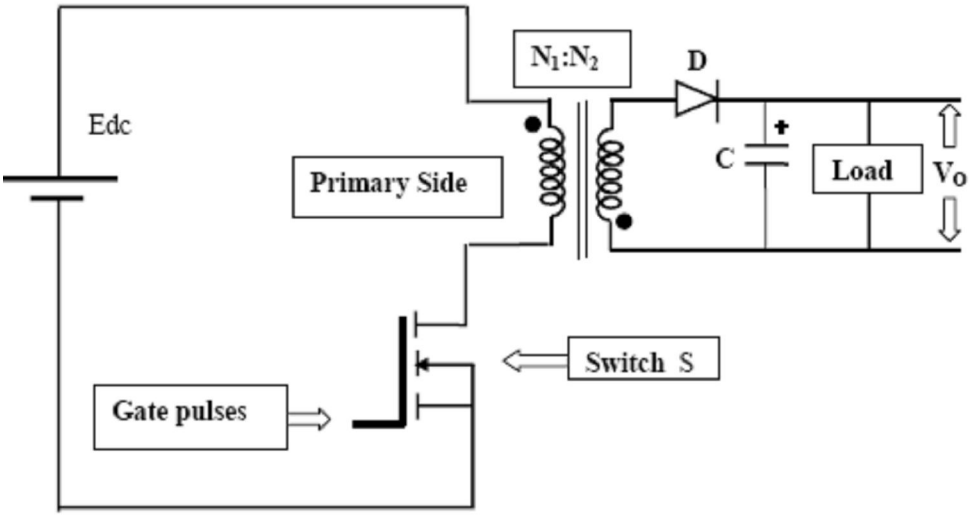


Figure-1: Fly-Back Converter Circuit

Linear rise of the primary current during the Mode-I is shown in Figure-3 (a) and (b). The Fly-Back circuit may have continuous flux operation (Continuous Conduction Mode CCM) or discontinuous flux operation (Discontinuous Conduction Mode DCM)-depicted in Figure 3a and b. In the case the circuit works in CCM the magnetic flux (or the primary current of inductor) is not reset to zero before the next cycle begins (i.e. again when MOSFET switch is turned ON). Since some flux is already present before MOSFET is turned ON, the primary winding current in Figure-3a abruptly rises to a finite value as the switch is turned ON. Magnitude of the current-step corresponds to the primary winding current required to maintain the previous flux in the core.

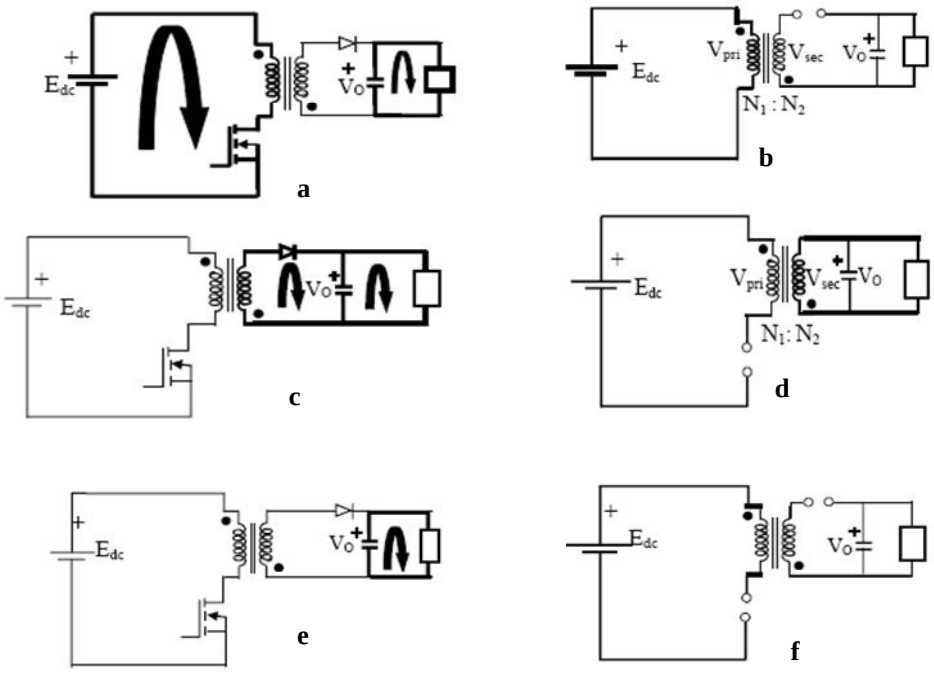
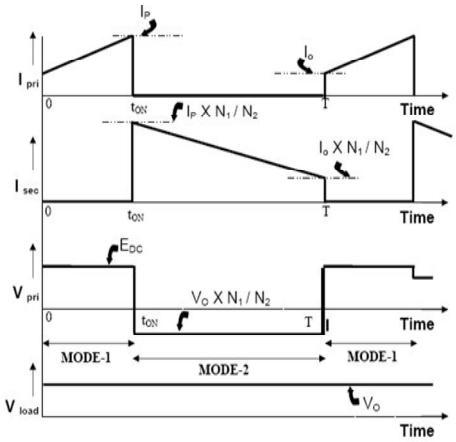


Figure-2: Modes I, II and III operations of Fly-Back Converter

At the end of switch-conduction (i.e. end of Mode-I), the energy stored in the magnetic field of the fly back inductor (transformer) is equal to $L_{pri}I_p^2/2$, where I_p denotes the magnitude of primary current at the end of conduction period. Even though the secondary winding does not conduct during this period or Mode-I, the load connected to the output capacitor gets uninterrupted current due to previously stored charge on the capacitor (steady-state operation). During the Mode-I assuming large capacitor the secondary winding voltage remains almost constant equals to $V_{sec} = E_{dc}\left(N_2/N_1\right)$. During Mode-I dotted end of secondary winding remains at higher voltage than the other end; under this condition, voltage stress across the diode connected to secondary winding (which is now reversed bias) is the sum of the induced voltage in the secondary and the output voltage ($V_{diode} = V_0 + E_{dc}\left(N_2/N_1\right)$).



a. CCM: Continuous Conduction Mode

b. DCM :Discontinuous Conduction Mode

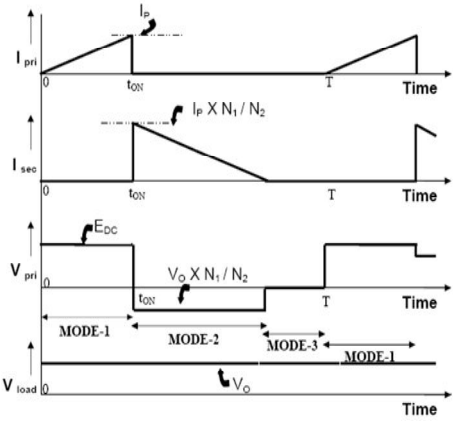


Figure-3: Continuous & Discontinuous Modes of Operation of Fly-Back Converter

Mode-II of circuit operation starts when the MOSFET switch is turned OFF after conducting for some time. The primary winding current path is broken and according to laws of magnetic induction, the voltage polarities across the winding reverse. Reversal of voltage polarities make secondary circuit's diode forward biased. The Figure-2c shows the current path (in bold lines) during this Mode-II, and Figure-2d shows equivalent circuit of this Mode-II. For the ideal circuit considered here, the secondary winding current abruptly rises from zero to $I_p\left(N_1/N_2\right)$ as soon as the MOSFET is turned OFF. This sudden rise is shown in Figure-3a and 3b. The diode connected in the secondary circuit allows only the current that enters the dotted end. The secondary current charges the output capacitor. The capacitor is large, so that its voltage doesn't change appreciably in a single switching cycle but over a period of several cycles that capacitor voltage builds up to its steady value. Capacitor voltage magnitude will stabilize if during each switching cycle the energy output by the secondary windings equals the energy delivered to the load. As can be seen from wave-forms of the Figure 3a and b; the secondary current decays linearly as it flow against the constant output voltage V_0, expressed as

$$L_{sec}\frac{\mathrm{d}i_{sec}}{\mathrm{d}t} = -V_0 \qquad i_{sec}(t) = -\frac{V_0}{L_{sec}}t + I_p\left(\frac{N_1}{N_2}\right) \tag{2}$$

Where L_{sec} and i_{sec} are the secondary winding inductance and current respectively; V_0 is stabilized magnitude of the output voltage; and $I_p\left(N_1/N_2\right)$ is the value of initial current at the start of Mode-II.

Under steady-state and under the assumption of zero ON-state voltage drop across diode; the secondary winding voltage during this mode equals V_0 and the primary voltage is $V_0\left(N_1/N_2\right)$; dotted ends of both windings being at lower potential. Under this condition voltage stress across MOSFET switch is sum of the induced voltage in primary and the DC supply voltage is $V_{switch} = E_{dc} + V_0\left(N_1/N_2\right)$. To this voltage V_{switch} there is a spike voltage added due to leakage inductive kick of the primary inductor-at the instant when the switch just opens; that is taken care by snubber circuit; so that MOSFET is saved-and this phenomena we will discuss later. Also there is high frequency ringing due to LC oscillations due to primary leakage inductance and stray capacitance. This oscillation will discuss later while developing the concept of Quasi-Resonant Valley Switching.

The secondary winding while charging the output capacitor (and feeding the load), starts transferring energy from the magnetic field of the fly back transformer to the power supply output in electrical form. If the OFF period of the switch is kept large, the secondary current gets sufficient time to decay to zero and magnetic field energy is completely transferred to the output capacitor and load. Flux linked by windings remains zero until next turn-ON of the MOSFET; and circuit is under discontinuous flux mode of operation (DCM). Alternatively if the OFF period of the MOSFET is small, the next turn-ON takes place before the secondary current decays to zero; the circuit is in CCM.

During the DCM after complete transfer of the magnetic field energy to the output, the secondary winding voltage as well as current falls to zero and the diode in series with the winding stops conducting. The output capacitor however continues to supply the uninterrupted voltage to the load. This part of the circuit is stated to be Mode-III, (Figure-2 e and f) of the circuit operation (only for DCM). Mode-III ends with the turn-ON of MOSFET switch and the circuit goes to Mode-I.

The Figure-3 gives ideal voltage and current wave-forms of the windings over a complete cycle. It may be noted that even though the two windings of the fly-back transformer do not conduct simultaneously they are still coupled magnetically (linking the same flux) and hence the induced voltages across the windings are proportional to turn ratio.

Circuit Equations under CCM

The waveform in Figure-3a corresponds to a steady state operation under CCM, with t_{ON} denoting the time for which the MOSFET switch is ON, during each switching cycle with T - as the time period of switching cycle. Let D be the duty cycle i.e. $D = t_{\mathrm{ON}}/T$. As seen from the Figure-3a, the primary current rises from I_0 to I_p in DT time. In terms of the input supply voltage E_{dc} and the primary winding inductance L_{pri}, we have following expression

$$\left(I_p - I_0\right) = \left(\frac{E_{dc}}{L_{pri}}\right)\left(DT\right) \tag{3}$$

Under the steady state the energy input to the primary winding during the each ON duration; i.e. $t=0$ to $t=t_{\mathrm{ON}}=DT$ is $\frac{1}{2}E_{dc}\left(I_p+I_0\right)\left(DT\right)$; written by following derivation

$$\int_{t_1}^{t_2} v_{pri}(t)i_{pri}(t)\mathrm{d}t=\int_{t_1=0}^{t_2=DT} E_{dc}i_{pri}(t)\mathrm{d}t;\qquad i_{pri}(t)=I_0+\left(\frac{E_{dc}}{L_{pri}}\right)(t),\qquad v_{pri}(t)=E_{dc}$$

$$=\int_0^{DT} E_{dc}\left(I_0+\tfrac{E_{dc}}{L_{pri}}t\right)\mathrm{d}t=\left[E_{dc}I_0t+\tfrac{E_{dc}^2t^2}{2L_{pri}}\right]_0^{DT}$$

$$=E_{dc}I_0\left(DT\right)+\frac{E_{dc}^2\left(DT\right)^2}{2L_{pri}}=\frac{1}{2}E_{dc}\left(\frac{2I_0L_{pri}+E_{dc}\left(DT\right)}{L_{pri}}\right)\left(DT\right)$$

$$=\frac{1}{2}E_{dc}\left(2I_0+\frac{E_{dc}}{L_{pri}}(DT)\right)(DT)=\frac{1}{2}E_{dc}\left(I_0+\left(I_0+\left(\frac{E_{dc}}{L_{pri}}\right)\left(DT\right)\right)\right)\left(DT\right)$$

$$=\frac{1}{2}E_{dc}\left(I_0+I_p\right)\left(DT\right);\qquad I_p=I_0+\frac{E_{dc}}{L_{pri}}DT$$

Similarly the output energy in each cycle is equal to $V_0I_{load}T$, where V_0 is output voltage magnitude, I_{load} is the load current. Equating these input and output energy (assume converter to be loss less) in each cycle, we get

$$\tfrac{1}{2}E_{dc}\left(I_p+I_0\right)\left(D\right)=V_0I_{load}\qquad(4)$$

The mean voltage (DC) across both primary and secondary winding must be zero under every steady state; this is volt-second area rule too. The average primary voltage in one cycle should be zero, means $\left\langle v_{pri}\right\rangle=\frac{1}{T}\int_0^T v_{pri}(t)\mathrm{d}t=0$ .When the MOSFET switch is ON the primary winding voltage equals input supply voltage, and when the MOSFET switch is OFF the reflected secondary voltage appears across the primary windings; now applying volt-second area criteria and under ideal diode and switch conditions we have

$$\left\langle v_{pri}\right\rangle_0^T=\tfrac{1}{T}\int_0^T v_{pri}(t)\mathrm{d}t=\tfrac{1}{T}\left(E_{dc}\left(DT\right)+\left(-V_0\left(\tfrac{N_1}{N_2}\right)\right)\left(\left(1-D\right)T\right)\right)=0$$

$$E_{dc}D=\left(N_1/N_2\right)V_0\left(1-D\right)\qquad(5)$$

The term $\left(N_1/N_2\right)V_0$ is the reflected secondary voltage across the primary windings (dotted end of the windings at lower potential) during Mode-II operation. Similarly $\left(N_2/N_1\right)E_{dc}$ is the induced voltage of secondary winding in Mode-I.

Thus we see for different E_{dc} , to have constant V_0, the duty ratio $D=t_{ON}/T$ modulates (5). Say when E_{dc} goes down, in order to maintain the constant V_0; the duty ratio D should increase. To increase duty ratio D for a constant switching frequency (T as a constant), on time of the switch i.e. t_{ON} should increase. Other way when, we want Constant-On-Time (COT) case i.e. t_{ON} is kept constant, when E_{dc}, goes down, to increase D , the T decreases; i.e. the switching frequency increases. When switch is OFF

it has to block a voltage which is V_{switch} in Mode-II; and when diode D is OFF in the Mode-I i.e. V_{diode} in Mode-I; are given below

$$V_{switch} = E_{dc} + V_0 \left(N_1 / N_2 \right) \qquad V_{diode} = V_0 + E_{dc} \left(N_2 + N_1 \right) \tag{6}$$

Circuit Equations under DCM

The Figure-3b shows wave-forms pertaining to DCM. During the Mode-III of the circuit operation primary and secondary winding currents as well as voltages are zero. The load however continues to get reasonably steady voltage due to relatively large output capacitor. With the turning ON of the MOSFET the primary winding current starts building up linearly from zero and at the end of Mode-I the magnetic energy due to the primary winding current is $\frac{1}{2} L_{pri} I_p^2$. The entire energy is transferred to the output at the end of Mode-II of circuit operation. Under loss-less assumption the output power is

$$P_0 = \frac{1}{2} L_{pri} I_p^2 f_{switch} \tag{7}$$

where $f_{switch} = \left(1/T \right)$ is the switching frequency of the converter It may be noted that output power is same as $V_0 I_{load}$ used in the equation (4) for CCM case. The volt-time area equation is used in equation (5) of CCM case gets modified under DCM case as

$$E_{dc} D \le \left(N_1 / N_2 \right) V_0 \left(1 - D \right) \tag{8}$$

Average voltage across winding over a switching cycle is still zero. The inequality in (8) is due to the fact that during the part of the OFF time period of MOSFET i.e. $\left(1-D\right)T$, the winding voltages are zero. This zero voltage duration is stated to appear in Mode-III. The equality sign of (8) will correspond to a just CCM case, which is boundary between CCM and DCM. The expressions (6) for V_{diode} and V_{switch} still holds for this DCM case too.

CCM versus DCM of Operation

A practical fly-back SMPS circuit has a close loop control circuit for output voltage regulation. The controller modulates the duty ratio of the switch to maintain the output voltage within small tolerable ripple around the set voltage. If the load is very light, very small amount of energy needs to be input to the circuit in each switching cycle. This is achieved by keeping ON duration of the switch low, resulting in very small duty ratio D. Within this small ON time only a small amount of current builds up in the primary winding. The OFF duration of the circuit operation which is (1-D) fraction of the switching time period, is relatively large. Thus at light loads the circuit is in Mode-III for significant duration. As the load increases the Mode-III duration, during which there is zero winding currents and zero flux through the core, reduces and the circuit is driven towards CCM. The circuit operation changes from DCM to CCM if the output power from the circuit increases beyond certain value. Similarly if the applied input voltage decreases keeping the load power and switching frequency constant the circuit tends to go to CCM. For better control of output voltage DCM is preferred. However for the given MOSFET transformers ratings; more output power can be transferred during CCM. A

common design thumb rule is to design the circuit for operation at just CCM at minimum expected input voltage (Boundary Conduction Mode BCM) and maximum rated output power.

Fly-Back Operation its Derivation and Analysis & Model

The fly-back converter is based on the buck-boost converter. We derive its functioning-the full circuit is depicted in Figure-4a; that is the basic buck-boost converter. When the MOSFET is ON, the source V_g gets connected to L making the current flow into the inductor; thus charging it. Due to this connection while MOSFET switch is ON the cathode point of diode D_1 is at higher potential, and thus the diode is reversed biased. When the MOSFET switch turns OFF, the polarity across the inductor reverses, due to theory of magnetic induction, making the cathode point of diode D_1 now at lower potential, making the diode forward bias. Now the inductor discharges its stored magnetic energy by charging the capacitor (when the MOSFET switch is OFF), with capacitor point connected to anode of diode as negative-the charged polarity is shown in Figure-4.

Figure-4b is same as Figure-4a here the inductor winding is spilt into two with turns ratio as 1:1, the basic function of the inductor is unchanged. Thus Figure-4a and 4b are equivalent. In Figure-4c we break the shorting link between the two windings of the 1:1 system, one winding is used while the transistor Q_1 conducts, while the other winding is used when the diode D_1 conducts. The total current in the circuit is unchanged from the circuit of Figure-4b. However, the current is distributed between the windings differently.

The magnetic fields in inside the inductor in both the cases are identical. Although the two-windings magnetic devise is represented using the same symbol as the transformer, a more descriptive name in this derivation will be “two winding inductor”. This device is sometimes called “fly-back transformer”. The Figure-4d is same as we discussed as classical circuit of Figure-1. Unlike the ideal transformer, current does not flow simultaneously in both the windings of the fly-back transformer. The transformer polarity marks are reversed in Figure-4d to obtain a positive output voltage. In order to generalize the concept, a $1:n$ turn’s ratio is introduced from 1:1 transformer-of Figure-4d. This Figure-4d is now same as classical circuit of Figure-1.

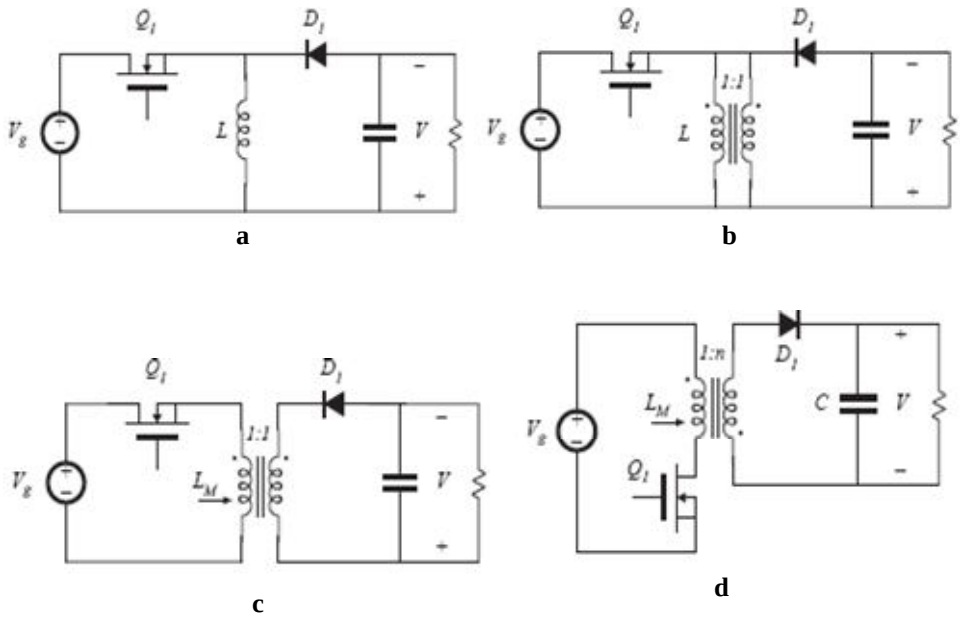


Figure-4: Fly-Back Converter derivation

The functioning of most transformer-isolated converters can be understood by modeling the physical transformer with simple equivalent circuit consisting of ideal transformer paralleled with the 'magnetizing inductance' L_M (Figure-5). The 'magnetizing inductance' L_M must then follow all the usual rules for inductors, in particular the volt-second area balance per switching cycle must hold when the circuit operates in steady state. This implies that the average voltage applied across every winding of the transformer must be zero.

Let us replace the transformer of Figure-4d with the equivalent circuit described above (i.e. with magnetization inductor)-that we depict in Figure-5a. The magnetizing inductance L_M functions in the same manner as inductor L of the original buck-boost converter of Figure 4a. When the MOSFET Q_1 conducts, energy from the DC source represented as V_g is stored in L_M; this is charging of inductor. When the diode D_1 conducts, this stored energy is transferred to the load, with the inductor voltage and current scaled by turn ratio that is $1:n$. During the sub-interval-1, as called Mode-I while the MOSFET Q_1 conducts the converter circuit model reduces to Figure-5b. The inductor voltage v_L, capacitor current i_C and the DC source current i_g are given by

$$v_L = V_g \qquad i_C = -\frac{v}{R} \qquad i_g = i \tag{9}$$

With the assumption that the converter operates with small inductor current ripple and small capacitor voltage ripple, the magnetizing current i and output capacitor voltage

v can be approximated by their DC components I and V respectively, and we re-write expression (9) as

$$v_L = V_g \qquad i_C = -\frac{V}{R} \qquad i_g = I \tag{10}$$

The average I is $\left\langle i_g \right\rangle_0^{DT_S} = \frac{1}{DT_S}\int_0^{DT_S} i_g(t)\mathrm{d}t$. Considering v_L as a constant in the time period DT_S, we have linear rise of inductor current $i(t) = \frac{V_g}{L_M}t$, assuming initial inductor current as zero. The maximum inductor current is $i_{\max} = \frac{V_g}{L_M}DT_S$, at the end of switch ON period. Thus the average current in the ON-period is

$$I = \frac{1}{DT_S}\int_0^{DT_S}\frac{V_g t}{L_M}\mathrm{d}t = \frac{1}{DT_S}\left[\frac{V_g t^2}{2L_M}\right]_0^{DT_S}$$

$$= \frac{1}{2}\left(\frac{V_g}{L_M}\right)\left(DT_s\right) = \frac{i_{\max}}{2}$$

We will use the above concepts in subsequent sections

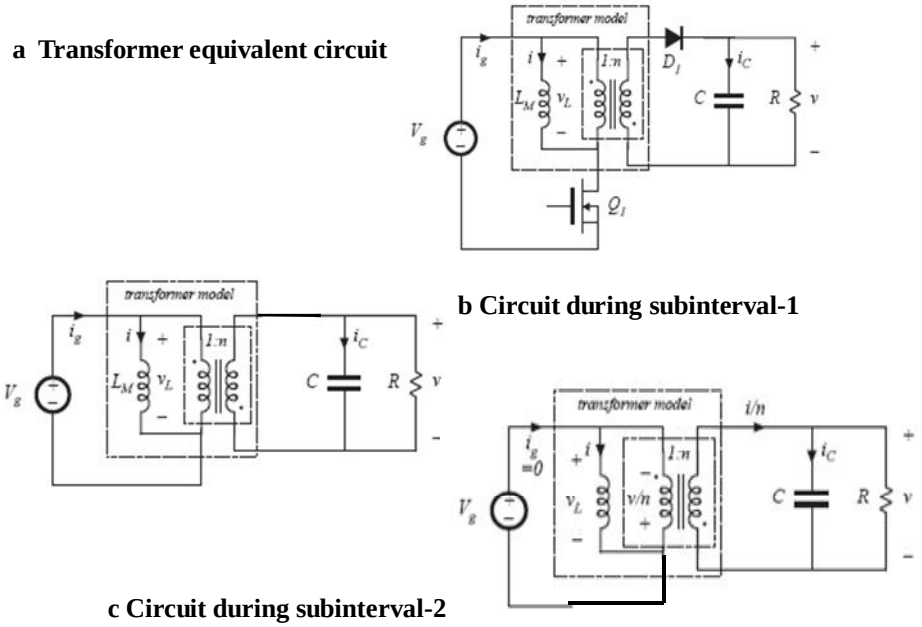


Figure-5: Fly-back converter circuit during operation at different subintervals

During the second subinterval (Mode-II) the MOSFET is in OFF state and the diode conducts. The equivalent circuit of Figure-5c is obtained. The primary-side magnetization inductance voltage v_L, the capacitor current i_C and the DC source current i_g for this sub-interval-2 (Mode-II) are

$$v_L = -\frac{v}{n} \qquad i_C = \frac{i}{n} - \frac{v}{R} \qquad i_g = 0 \tag{11}$$

It is important to consistently define $v_L(t)$ on the same side of transformer for all the subintervals (Modes). Upon making the small-ripple approximation as earlier we re-write the above as

$$v_L = -\frac{V}{n} \qquad i_C = \frac{I}{n} - \frac{V}{R} \qquad i_g = 0 \tag{12}$$

The $v_L(t)$, $i_C(t)$ and $i_g(t)$ are depicted in Figure-6; as average values. Note that in actual case i_g is linearly rising current in ON-time duration, but the figure show average i_g, a constant value as I. Application of volt-second balance to primary side magnetization inductor gives-average v_L as zero, i.e.

$$\langle v_L \rangle = D(V_g) + D'\left(-\frac{V}{n}\right) = 0 \qquad D' = 1 - D \tag{13}$$

Solution for the conversion ratio from above yields following same as was discussed in expression (5) in previous section

$$M(D) = \frac{V}{V_g} = n\frac{D}{D'} \tag{14}$$

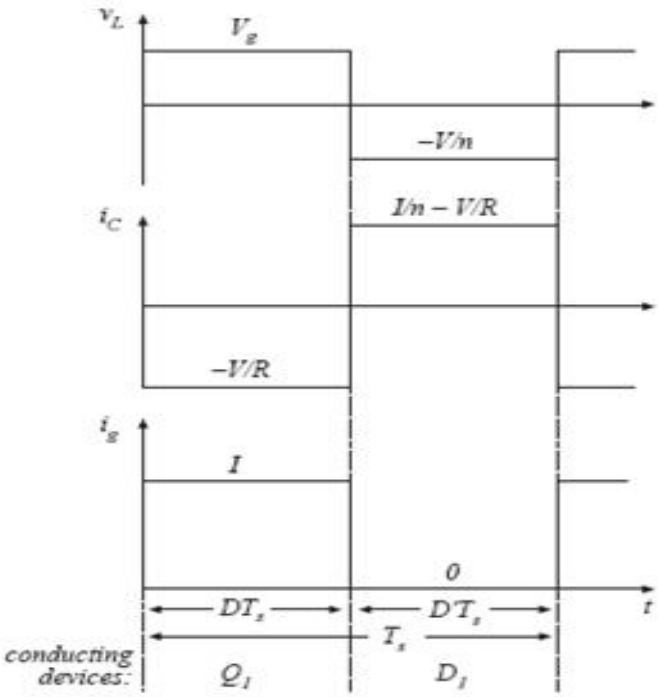


Figure-6: Fly-Back Converter Average or DC Wave-Forms Continuous Conduction Mode

So the conversion ratio of the fly-back converter is similar to that of buck-boost converter with added factor as turn ratio. Application of charge balance to the output capacitor leads following (i.e. $\langle q_C \rangle$ -is average charge in one switching cycle is zero)

$$\langle q_C \rangle = DT\left(-\frac{V}{R}\right) + D'T\left(\frac{I}{n} - \frac{V}{R}\right) = 0 \qquad D' = 1 - D \tag{15}$$

This gives

$$I = \frac{nV}{D'R} \tag{16}$$

This is DC component of the magnetization current, referred to primary side. This expression says that for a LED as load, the R is the total dynamic resistance of LED, and V, the output voltage of LED string is also constant. Thus for a set LED current I_{LED}; we get fixed duty ratio D. The DC component of the source current i_g is

$$\langle i_g \rangle = I_g = D(I) + D'(0) \tag{17}$$

From (17) we get average input current

$$\langle i_g \rangle = I_g = D(I) = \frac{1}{2}\left(\frac{V_g}{L_M}\right)\left(D^2 T_s\right) = \frac{i_{\max}}{2} D$$

An equivalent circuit which models the DC component of the fly-back converter waveforms we know construct. The resulting DC equivalent circuit of the fly-back converter is depicted in Figure-7. It contains a $1:D$ buck-type conversion ratio followed by a $(1-D):1$ boost-type conversion ratio, with an added factor $1:n$ arising from fly-back transformer turns-ratio.

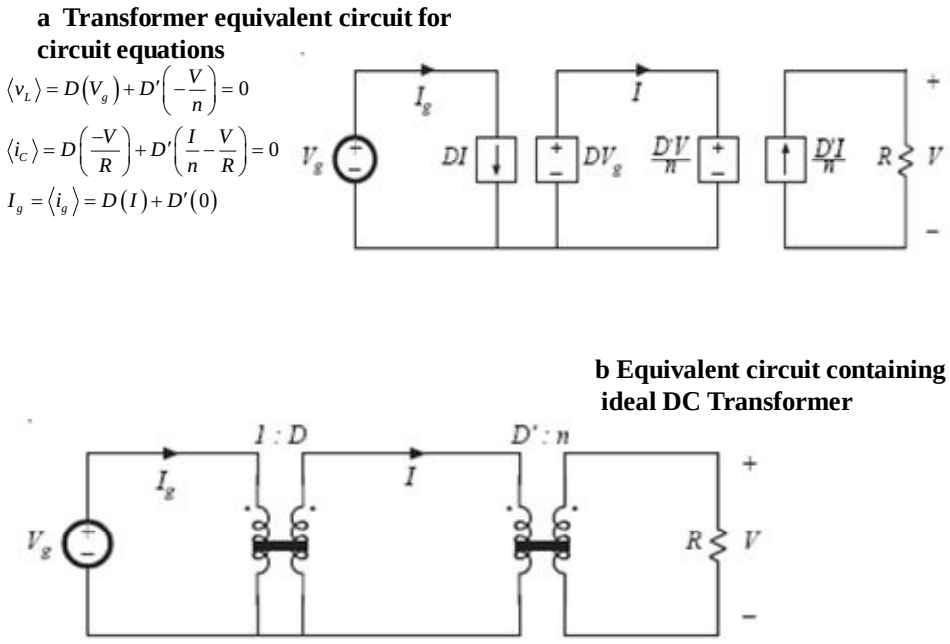


Figure-7: Fly-Back Converter Equivalent Circuit Model Buck-Boost System

The peak transistor (MOSFET) voltage is equal to the DC input voltage V_g plus the reflected load voltage V/n,(in practice, additional voltage is observed due to ringing associated with the transformer leakage inductance-that we will discuss in subsequent

section). A snubber circuit may be added to clamp the magnitude of this ringing voltage to a safe value that is within the peak voltage rating of MOSFET.

The Snubber Circuit

The snubber circuit consists of a fast recovery diode in series with parallel combination of a snubber capacitor and a resistance. The leakage inductance current of the primary winding finds a low impedance path through the snubber diode to snubber capacitor. It can be seen that the diode end of the snubber capacitor will be at higher potential. To check the excessive voltage builds up across the snubber; capacitor and resistor is put across it. Under steady state this resistor is meant to dissipate the leakage flux energy. The power lost in the snubber circuit reduces overall efficiency of the fly-back type SMPS circuit. In order that snubber capacitor does not take away any portion of energy stored in the mutual flux of the windings, the minimum steady state snubber capacitor voltage should be greater than reflected secondary voltage on the primary side. This can be achieved by proper choice of snubber resistor and keeping RC time constant of the snubber circuit significantly higher than the switching time period. Since the snubber capacitor voltage is kept higher than the reflected secondary voltage, the worst case MOSFET switch voltage stress will be sum of input voltage and the peak magnitude of snubber capacitor voltage.

The leakage inductance L_l is effectively in series with MOSFET (See Figure-8). When MOSFET switches OFF (at time DT_S) it interrupts the current flowing through L_l, this L_l induces a voltage spike according to $v_l(t) = L_l\left(\mathrm{d}i_l / \mathrm{d}t\right)$. This spike voltage will appear extra to the OFF voltage of MOSFET i.e. as we discussed is $V_g + \left(V / n\right)$, while MOSFET switches OFF at the end of Mode-I. Thus the peak voltage appearing at the switch OFF instant of MOSFET is $L_l\left(\mathrm{d}i_l / \mathrm{d}t\right) + V_g + \left(V / n\right)$; if this exceeds the rating, then MOSFET will fail. Thus snubber provides a path for i_l to flow after MOSFET switch has turned OFF. Energy stored in the leakage inductance $\frac{1}{2}L_l i_l^2 = \frac{1}{2}L_l I^2$ is transferred to C_S and dissipated by R_S.

The average power is $\frac{1}{2}L_l I^2 f_S$, (where $f_S = 1/T_S$; is MOSFET switching frequency) and peak MOSFET voltage gets clamped to $V_g + v_S > V_g + \left(V / n\right)$. As an approach to select C_S and R_S, use large C_S, so that $v_S(t)$ has negligible ripple. That is $R_S C_S \gg T_S$. This implies $v_S(t) \approx V_S$; that is DC; this is ripple free approximation. Voltage V_S rises until power dissipated by R_S is equal to the average power transferred from L_l, i.e. $V_S^2 / R_S = \frac{1}{2}L_l I^2 f_S$. Choose R_S such that V_S is acceptably low. We note here that L_l depends on winding geometry and is not known until transformer is wound, so measure L_l by short circuit test, or guess its value.

Let us work for an example. Given say $V_g = 150\text{V}$, $V = 15\text{V}$, $1:n = 1:0.2$, $f_S = 100\text{KHz}$, $L_M = 1\text{mH}$, $I = 1.5\text{A}$. MOSFET peak voltage rating is 400V. It is desired to limit peak (say V_T) to 325V. A good estimate for a carefully wound transformer it may be possible to have L_l as 3% of $L_M = 1\text{mH}$ i.e. $L_l = 30\mu\text{H}$. We take value of $L_l = 30\mu\text{H}$, for our calculations. Thus energy stored in L_l, during the ON time $0 < t < DT_S$, is $W_l = \frac{1}{2} L_l I^2$; that is $\left(\frac{1}{2}\right)\left(30\mu\text{H}\right)\left(1.5\right)^2 = 33.75\mu\text{J}$. Average power transferred from L_l to snubber is $P_l = W_l f_S$, which is $\left(33.75\mu\text{J}\right)\left(100\text{KHz}\right) = 3.375\text{W}$. To limit MOSFET transistor voltage V_T to 325V, we need $V_S = (\text{peak} - V_T) - V_g = 325\text{V} - 150\text{V}$, i.e. 175V. So we get $R_S = V_S^2 / P_l$ as $R_S = \left(175\text{V}\right)^2 / (3.375\text{W}) = 9047\Omega$. We choose $R_S = 10\text{k}\Omega$. Then $C_S \gg T_S / R_S$; gives $C_S \gg \left(10\mu\text{s}\right) / \left(10\text{k}\Omega\right) = 1\text{nF}$; can choose $C_S = 47\text{nF}$.

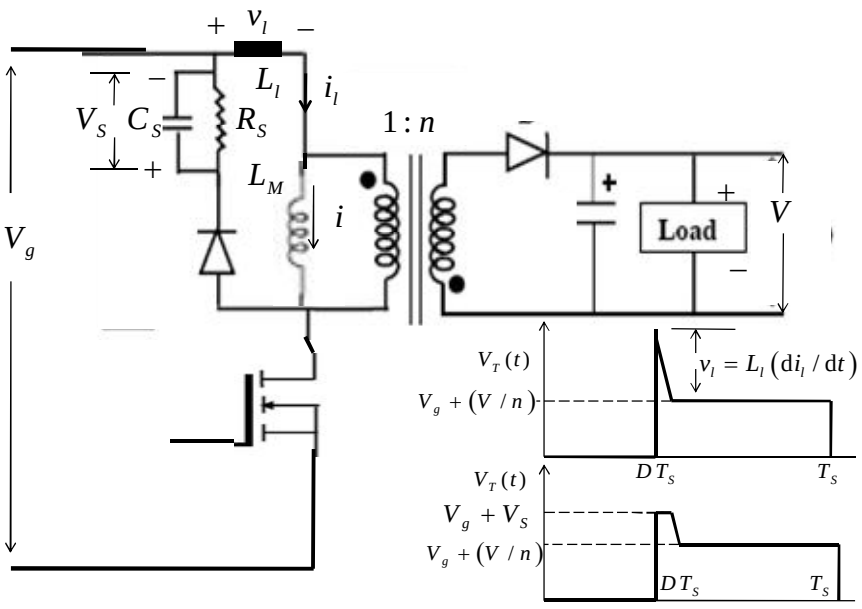


Figure-8: Use of SNUBBER Circuit

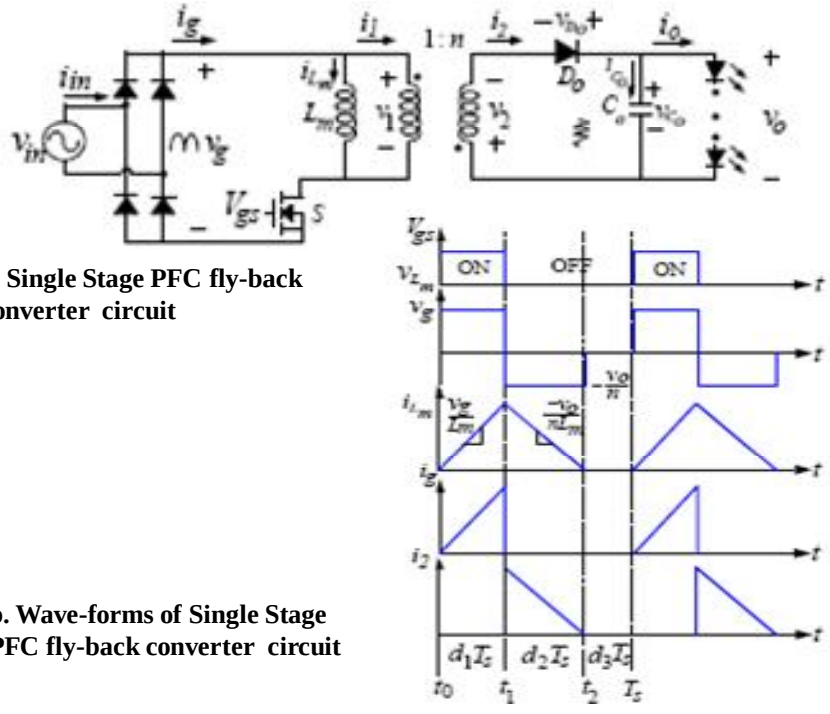
In the above Figure-8, the spike due to leakage inductance is also associated by high frequency ringing due to resonance formed by the leakage inductance and stray MOSFET drain node capacitance. That ringing is not shown in this figure-will be taken up later, while discussing Quasi Resonant Valley Switching.

Transformer Isolated Fly-back Converter Circuit with Power Factor Correction (PFC) with Constant Frequency Switching

What ever fundamental discussions we had in earlier sections; now we try to use these concepts to have some practical circuits in the subsequent sections to drive LED bulb.. A

DC/DC converter that provides isolation between the rectified AC line source and LED string is the fly-back circuit of Figure-9a. The dot convention is used to indicate relative polarity between the primary winding and the secondary winding. The energy storage capacitor on the primary-side of the fly-back transformer is removed. The voltage v_g is full-wave sinusoidal voltage rectified from power AC line v_{in}. The component L_m denotes magnetization inductance of the fly-back transformer (with turn ratio $1:n$).

The input energy is stored in L_m when the MOSFET power switch S is ON and then transferred to the load when the switch is OFF. The energy storage capacitor C_0 is the bulk capacitor to provide a smooth DC link voltage for LED. The fly-back converter can operate in Continuous Conduction Mode CCM or Discontinuous Conduction Mode DCM with respect to current continuity. Since the switch S is switched ON and switched OFF at high frequency, the input current becomes pulsating wave-form at the same frequency. By proper control the amplitude & duration of the pulsating current, the average of the input current can be made sinusoidal and in phase with the input voltage. Consequently, a near unity power factor and a very low THD are achieved. Besides the fly-back converter operating in DCM with constant frequency and fixed duty-cycle utilizes far fewer components than traditional two-stage approach. This is basic single stage approach-employing Transformer Isolation-operating in fixed duty cycle and constant frequency.



a. Single Stage PFC fly-back converter circuit

b. Wave-forms of Single Stage PFC fly-back converter circuit

Figure-9: Single-stage Transformer Isolated fly-back converter and its wave-forms

Assumptions are: 1) All the circuit components are ideal, 2) The switching frequency is much higher than AC line 50Hz; thus input voltage is considered as constant during the switching cycle, 3) The energy store capacitor C_0 is sufficiently large this makes output voltage v_0 as ideal DC voltage, 4) We consider steady state for the circuit so that all voltage and currents are

periodic, beginning and ending at the same points over one switching cycle. The wave-form of the circuit is shown in Figure-9b. We assume that turn ratio $1/n$ of the fly-back transformer is greater than one.

Calculations for Transformer Isolated fly-back converter in one switching cycle of constant frequency and fixed duty ratio

We start with Mode-I-i.e. time when $t_0 < t < t_1$ (Figure-9b). At the instant t_0 the switch is ON and energy transfer diode D_0 is OFF. The circuit loop around contains the rectified voltage source, magnetization inductor, and closed switch is depicted in Figure-10a.The fly back converter is supplied from AC line voltage source that is

$$v_g = |v_{in}(t)| = V_m \left|\sin\left(2\pi f_L t\right)\right| \tag{18}$$

Where f_L is the line frequency 50Hz and V_m is the peak amplitude of AC input voltage. In order to turn ON the MOSFET at zero current, the circuit is designed to operate in DCM. When the power-switch S is turned ON, the rectified line source voltage is applied on the magnetization inductor. The magnetization current rises linearly (1) from zero (i.e. at $t = t_0$) with a slope proportional to instantaneous AC line voltage, and is given by

$$i_{L_m}(t) = \left(\frac{V_m}{L_m}\left|\sin\left(2\pi f_L t\right)\right|\right)(t - t_0), \qquad t_0 < t < t_1 \tag{19}$$

The above is from $i_{L_m}(t) = \frac{1}{L_m}\int_{t_1}^{t} |v_{in}(t)|\mathrm{d}\bar{t}$; with $v_{in}(t)$ taken as constant in the switching time interval; in (1) $E_{dc} = |v_{in}(t)| = V_m \left|\sin\left(2\pi f_L t\right)\right|$ .The switching frequency f_S of fly-back converter is designed to be much higher than the line frequency f_L, therefore the input AC line voltage can be regarded as constant during one switching cycle. The peak current in each high frequency cycle is (obtained at $t = t_1$), meaning $t_1 - t_0 = d_1 T_S$, given as following

$$i_{L_m,peak} = \left(\frac{V_m}{L_m}\left|\sin\left(2\pi f_L t\right)\right|\right)\left(d_1 T_S\right) \tag{20}$$

In this mode, the input current i_{in} i.e. $i_g(t)$ is equal to $i_{L_m}(t)$. The energy transfer diode D_0 is turned OFF by the negative polarity of $nv_g + V_0$. From Figure-10a, the voltage across the energy transfer diode D_0 is obtained by

$$v_{D_0} = -(nv_g + V_0) \tag{21}$$

$$v_1 = v_g \qquad v_2 = nv_g \tag{22}$$

$$i_2 = 0 \tag{23}$$

$$i_1 = ni_2 = 0 \tag{24}$$

In this interval the up-slope of the i_{L_m} is $\frac{V_m|\sin(2\pi f_L t)|}{L_m}$; the slope is steep, if V_m is higher and so is $i_{L_m,peak}$ for constant $d_1 T_S$ or Constant -ON Time (COT) for MOSFET.

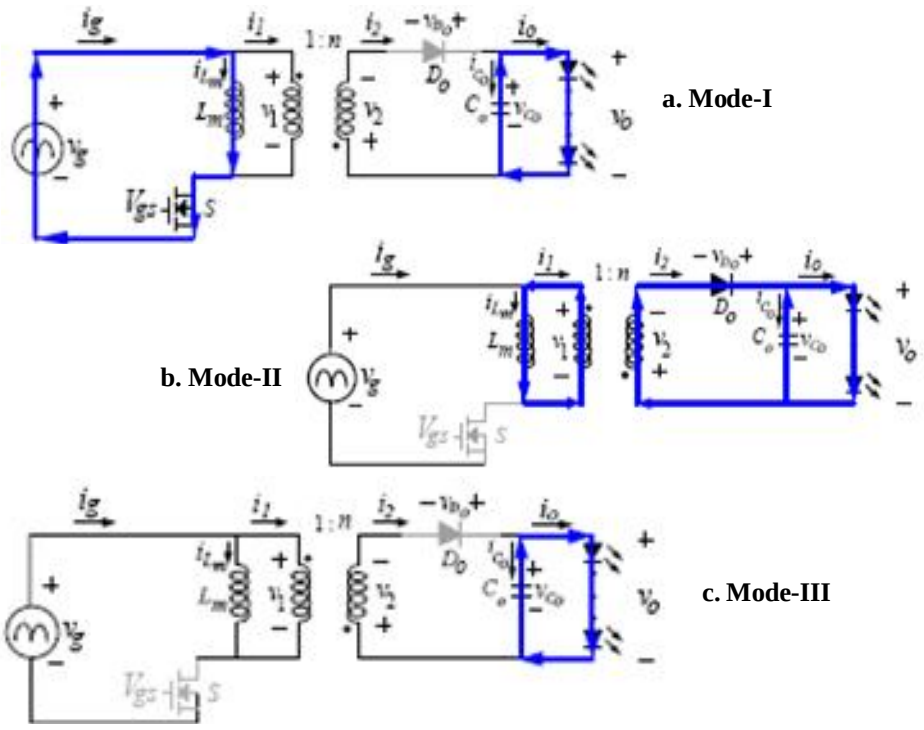


Figure-10: Modes of operation in one switching cycle and corresponding equivalent circuits

During the ON period energy is stored in the magnetizing inductor and that gets transferred to the output side during the OFF period of the switching cycle.

The Mode-II (equivalent circuit is depicted in Figure-10b) is in time period $t_1 < t < t_2$. At $t = t_1$, the switch S is turned OFF, forcing the energy transfer diode D_0 to conduct and to carry the reflected current through the secondary winding of the fly-back transformer. At the instant, the input current, i_{in} i.e. i_g becomes zero, constraining i_{L_m} to go through the primary windings of the transformer. The output current i_2 of the secondary side of the transformer flows through the energy transfer diode D_0. The voltage across the output terminal of the fly-back transformer is V_0. Hence transformer primary side voltage V_1 is following

$$v_1(t) = \frac{v_2(t)}{n} = \frac{-V_0}{n} \tag{25}$$

When $t = t_1$ the switch S is turned OFF, the energy transfer diode D_0 is turned ON and the energy stored in magnetization inductor is delivered to the energy storage capacitor C_0. During this period $t_1 < t < t_2$, the magnetizing inductor current decreases linearly. Therefore we write following expression

$$i_{L_m}(t) = \frac{-\frac{V_0}{n}}{L_m}(t - t_1) + i_{L_m, peak} \tag{26}$$

In this discharge interval the down-slope of i_{L_m} is $\left(\frac{V_0}{nL_m}\right)$; we see this down-slope does not depend on the V_m. Thus for constant output V_0 the down-slope is always at same rate of fall (Figure-9b). Meanwhile, the energy stored in the magnetizing inductor of the fly-back converter is released to the energy storage capacitor C_0. The time $t_2 - t_1 = d_2 T_S$ (Firure-9b) needed for magnetizing inductor current i_{L_m} to go to zero. It can be calculated by substituting (20) and (25) into (26), and is expressed in (27).

$$0 = \frac{-\frac{V_0}{n}}{L_m} d_2 T_S + i_{L_m,peak} \qquad i_{L_m,peak} = \left(\frac{V_m}{L_m}\left|\sin\left(2\pi f_L t\right)\right|\right)\left(d_1 T_S\right)$$

$$d_2 T_S = \frac{i_{L_m,peak}}{\frac{\left(\frac{V_0}{n}\right)}{L_m}} = \frac{V_m\left|\sin\left(2\pi f_L t\right)\right|}{\left(\frac{V_0}{n}\right)}\left(d_1 T_S\right) \tag{27}$$

This mode ends when i_{L_m} becomes zero. Though i_{L_m} becomes zero at time $t - t_1 = d_2 T_S$, the next switching ON of the MOSFET is done after some time delay i.e. $d_3 T_S$. This gives in addition the energy transfer diode D_0 is turned OFF under zero current condition without reverse recovery loss.

If we have constant $d_1 T_S$; i.e. the ON-time for MOSFET, from (20), we see that for lower V_m, we will get lower $i_{L_m,peak}$ and also a less steep 'up-slope' while inductor is charging. With this Constant-On-Time (COT) system, we also infer that time to take current i_{L_m} to go to zero i.e. $d_2 T_S$ will be lesser for lesser V_m; though the rate of fall (the down-slope of i_{L_m}) in Mode-II will always be same. For a constant switching frequency T_S as constant we see for a lesser V_m the time $d_3 T_S$ will be larger. In a way for constant load V_0 as constant a COT system with fixed switching frequency will be operating at DCM at lower V_m and with increase in V_m the circuit would be tending to operate in BCM-but never to CCM. This is how one should select the components for minimum input voltage to maximum input voltage and for constant LED output voltage and LED current.

Mode-III (Figure-10c) is at $t_2 < t < T_S$; with power switch S as OFF. Here the energy transfer diode D_0 is OFF; the current of fly-back transformer output terminal is zero. During this mode, only a load current i_0 flows through the energy storage capacitor C_0. Voltages and currents for an open switch are

$$v_1 = 0 \tag{28}$$

$$v_2 = 0 \tag{29}$$

$$i_0 = \frac{v_0}{R} \tag{30}$$

When the switch S is excited again by the gate-drive signal V_{gs}, this mode ends and the circuit operation returns to Mode-I. At the end of Mode-III (only for DCM) the switching

ON of MOSFET is at zero voltage, and zero current; this is minimizing the switching losses, and thereby increasing the circuit efficiency.

During the Mode-I and Mode-II the AC line source supplies current to the single-switch fly-back converter stage. The unfiltered input current $i_{in}(t)$ is equal to $i_g(t)$, which is $i_{L_m}(t)$ in Mode-I ($t_0 < t < t_1$); and is zero i.e. $i_{in}(t) = i_g(t) = 0$; for Mode-II; i.e. ($t_1 < t < t_2$). Because the single switch fly-back converter stage is operated at DCM over an entire line frequency cycle (50Hz), the current i_g (we say i_{L_m}) increases from zero at the beginning of Mode-I; then it suddenly drops to zero at the instant $t = t_1$, see plot of i_g and circuit (Figure-9b and 10b the i_g drops to zero i.e. $i_g = 0$ at $t = t_1$). The current waveform of magnetizing inductor L_m in a complete utility line cycle (50Hz) is shown in Figure-11. Its peak as calculated in (20) is

$$i_{L_m,peak}(t) = i_{g,peak}(t) = \left(\frac{V_m}{L_m}\left|\sin\left(2\pi f_L t\right)\right|\right)\left(d_1 T_S\right) = \left(\frac{V_m\left|\sin\left(2\pi f_L t\right)\right|}{L_m f_S}\right)\left(d_1\right)$$

Where $\left|V_m \sin\left(2\pi f_L t\right)\right|$ is instantaneous line voltage which can be considered as constant within each switching cycle. We represent average $I_{L_m,avg}(t)$, charging current as following, by taking the average in the ramping time interval $t_0 < t < t_1$, or $0 < \bar{t} < d_1 T_S$

$$\begin{aligned} I_{L_m,avg}(t) &= \frac{1}{d_1 T_S}\int_0^{d_1 T_S} \frac{\left|V_m \sin\left(2\pi f_L t\right)\right|}{L_m}\bar{t}\left(\mathrm{d}\bar{t}\right) = \frac{1}{d_1 T_S}\frac{\left|V_m \sin\left(2\pi f_L t\right)\right|}{L_m}\left(\frac{(d_1 T_S)^2}{2}\right) \\ &= \frac{\left|V_m \sin\left(2\pi f_L t\right)\right|}{2L_m}\left(d_1 T_S\right) = d_1\frac{\left|V_m \sin\left(2\pi f_L t\right)\right|}{2L_m f_S} \\ &= \frac{i_{L_m,peak}(t)}{2} \end{aligned} \tag{31}$$

This we have derived too in previous section.

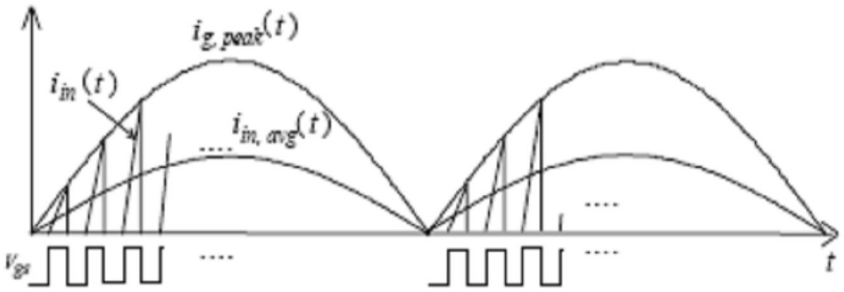


Figure-11: Rectified Input Current Wave-form of the Fly-Back Converter

The average value of input current $i_{in,avg}(t)$ within a high frequency switching period can be calculated as following

$$i_{in,avg}(t) = i_{g,avg}(t) = \frac{1}{T_S}\int_{t_0}^{t_2} i_g(\bar{t})\mathrm{d}\bar{t} = \frac{1}{T_S}\left(\int_{t_0}^{t_1} i_{L_m}(\bar{t})\mathrm{d}\bar{t} + \int_{t_1}^{t_2}(0)\mathrm{d}\bar{t}\right)$$

$$= \frac{1}{T_S}\int_0^{d_1T_S} \frac{\left|V_m \sin(2\pi f_L t)\right|}{L_m}(\bar{t})\mathrm{d}\bar{t} = \frac{1}{T_S}\left[\frac{\left|V_m \sin(2\pi f_L t)\right|}{L_m}\left(\frac{(\bar{t})^2}{2}\right)\right]_0^{d_1T_S} \tag{32}$$

$$= \frac{\left|V_m \sin(2\pi f_L t)\right|}{2L_m}\left(d_1^2 T_S\right) = \frac{i_{L_m,peak}(t)}{2} d_1$$

The above too we have derived earlier. Defining the following terms-i.e. equivalent resistance of the fly-back converter R_e as

$$R_e = \frac{2L_m}{d_1^2 T_S} \tag{33}$$

We get the current flowed into the fly-back converter during Mode-I interval $t_0 < t < t_1$, and Mode-II; with $v_g = \left|V_m \sin(2\pi f_L t)\right|$ is

$$i_{in,avg}(t) = i_{g,avg}(t) = \frac{v_g(t)}{R_e} \tag{34}$$

The above expression (32) reveals that the average input current is sinusoidal and in phase with AC line voltage $v_g(t) = V_m \sin(2\pi f_L t)$, provided that R_e is a constant (possible if and only if $d_1^2 T_S$ is kept constant) . Thus, as the single switch fly-back converter for PFC stage is designed to operate at DCM with fixed switching frequency T_S and constant ON time $d_1 T_S$, the input current naturally follows a sinusoidal waveform of the AC line source. In other words if f_S, the switching frequency remains constant, with D as duty ratio i.e. $D = \frac{d_1}{d_2+d_3} = \frac{t_{ON}}{t_{OFF}}$ fixed, we get unity power factor. These results a high power factor of utility line-the rectified current waveform $i_{g,avg}(t)$ of the AC line in a complete line cycle 50Hz is shown in Figure-11.

The power absorbed by the single stage PFC circuit with fly-back converter from the source during a half line cycle is equal to the power absorbed by the string of LED's at the same time

$$\eta P_{in} = P_0 \tag{35}$$

Where η is the circuit efficiency. Considering loss less system with $\eta = 1$ that is

$$\frac{1}{T_L}\int_0^{T_L} v_g(t) i_g(t)\mathrm{d}t = \frac{v_0^2}{R} \tag{36}$$

Where T_L says the time period of the rectified line source, v_0 and R are the output voltage and load resistance (total dynamic resistance of LED string) of the fly-back converter for LEDs lighting application. Based on loss-less concept ($\eta = 1$) of power balance we write the following.

$$\frac{v_{in}^2}{R_e} = \frac{v_0^2}{R} \tag{37}$$

Using $R_e = \left(2L_m\right)/\left(d_1^2 T_S\right)$ from (33); substituting above, and using $V_m = v_{in}/\sqrt{2}$ we get

$$d_1 = \frac{v_0}{v_{in}}\sqrt{\frac{2L_m}{RT_S}} = \frac{v_0}{V_m}\sqrt{\frac{L_m}{RT_S}} \tag{38}$$

However the sum of the duty ratios should be less than unity to ensure DCM operation in this fly-back circuit that is

$$d_1 + d_2 < 1 \tag{39}$$

We apply volt-second area relationship to the magnetizing inductor voltage at primary side to write following

$$d_1 v_g + d_2\left(-\frac{v_0}{n}\right) = 0 \tag{40}$$

From (39) and (40) we get

$$d_1 < \frac{1}{1+\frac{nv_g}{v_0}} \tag{41}$$

For the worst case when $v_g = V_m$; we write

$$d_1 < \frac{1}{1+\frac{nV_m}{v_0}} \tag{42}$$

Using the relation $v_1 = \frac{v_2}{n} = -\frac{V_0}{n}$, and $d_1 = \frac{v_0}{V_m}\sqrt{\frac{L_m}{RT_S}}$, we get

$$L_m < \frac{RT_S}{\left(1+\frac{V_0}{V_m}\right)^2} \tag{43}$$

Fly-back Converter Circuit without Transformer Isolation for PFC with using Quasi-Resonant Valley Switching

We have seen the use of $1:n$ fly-back transformer in the classical converter, and derived the way of having input current follow the input voltage by deliberately maintaining constant duty ratio and switching frequency; and derived essential expressions. The LED driver circuit using this classical concept as described previously, have many advantages; their efficiencies are of the order 80%. Now we discuss a topology for LED bulb application for usually less than 25W, the circuit that we will discuss is operated at Boundary Conduction Mode (BCM) and DCM. The high power factor is achieved here by Constant-On-Time (COT) control, in both BCM and DCM operations; but with variable frequency as with input voltage.

In order to enhance the circuit efficiency Quasi-Resonant (QR) valley switching is one modern method that is achieved by L-C resonant tank, which comprises of main inductance and the parasitic capacitance of the MOSFET. In a way the MOSFET will be

switched ON once drain-source voltage resonates to the lowest value minimizing the switching loss, and this method is called valley switching. Also we shall be using one inductor instead of a transformer as described in previous sections. Figure-12 is the basic circuit of the buck-converter.

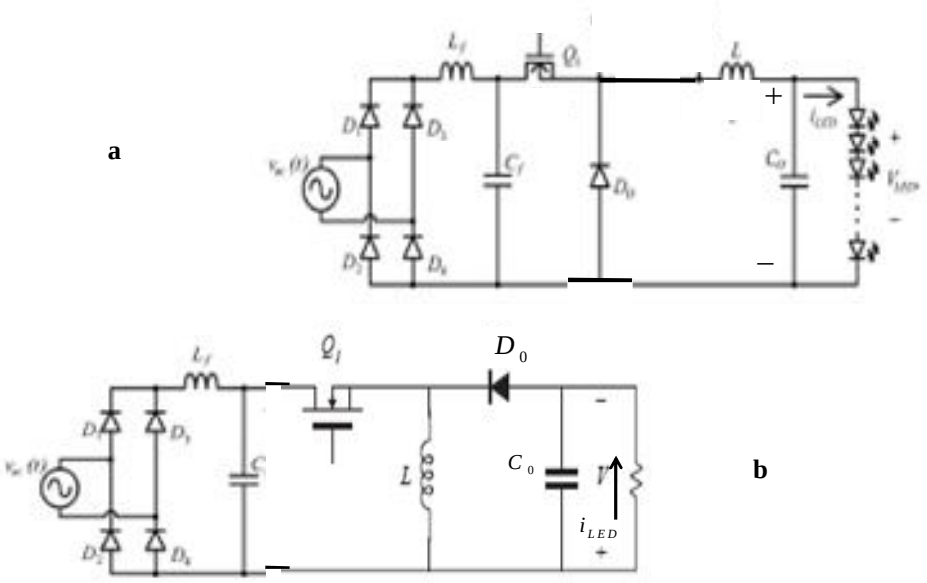


Figure-12: Configuration of buck-converter with one-inductor

The Figure12a we will use in this section and Figure-12b is to show that it is same as was the original circuit of buck-boost converter of Figure-4a; from where we derived the classical buck-boost converter with $1:n$ fly-back transformer. We redraw the circuit of Figure-12a with R_{CS} that is to measure the inductor current to have QR valley switching; and for setting the LED current. In Figure-13, we see one end of the R_{CS} is marked as V_{SS} ; this point is the signal ground (or floating ground) reference point, with respect to this point the measurements for inductor current and subsequent switching of MOSFET is carried out. The feed-back circuits as depicted in Figure-17 and 18 and the detection of QR valley points is referred to this signal ground point V_{SS} ; whereas the power ground is separate as shown in Figure-13 by a conventional symbol of ground point.

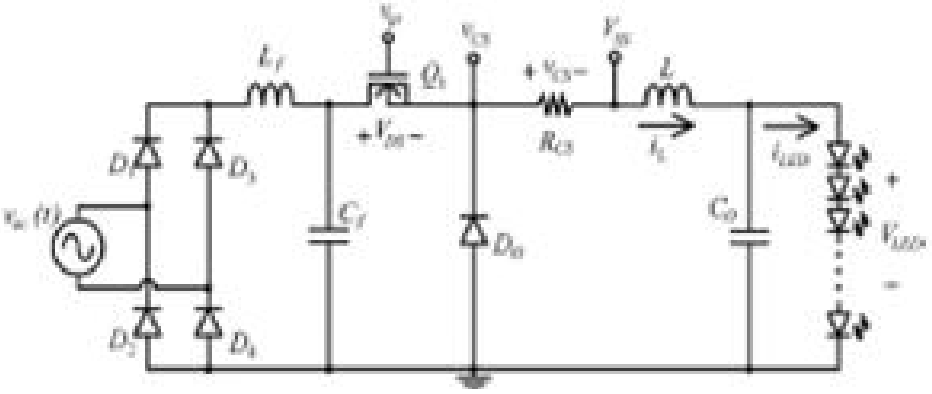
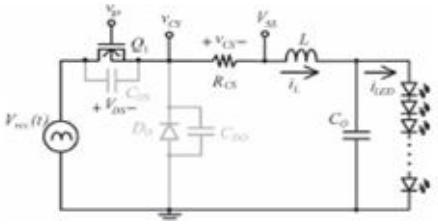
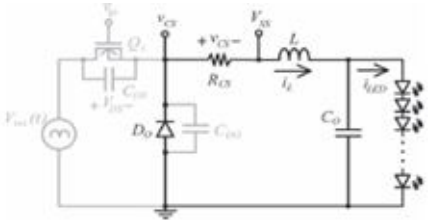


Figure-13: Buck converter circuit for LED drive

a-Mode-I operation





b-Mode-II operation

c-Mode-III operation

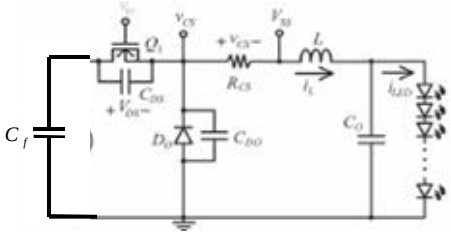


Figure-14: Modes of operation of the circuit

The full circuit is in Figure-13. Figure-14 and 15 describes the operating equivalent circuit and theoretical waveforms respectively. For simplicity the line voltage source the diode bridge rectifier and EMI filter ($L_f - C_f$) are replaced by an equivalent line

voltage V_{rec}. The steady state operation is explained by three modes within one switching cycle. The v_{CS} signal (when going negative) is used to detect the instant when switching ON is to be done for MOSFET-(is QR Valley Switching). The v_{CS} is voltage across the sense resistor R_{CS}; the voltage is measured with respect to V_{SS} the floating ground.

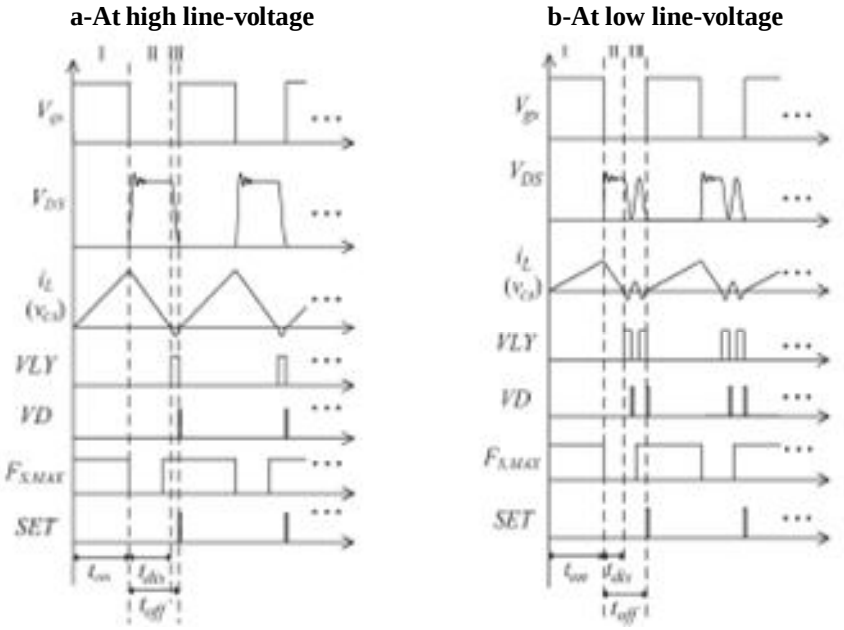


Figure-15: Theoretical wave-forms

When v_{CS} (indicating the inductor current) is negative, there is a comparator to detect QR valley detector circuit. That comparator outputs a signal VLY; (Figure-17 and 18). This signal VLY is sent to the negative edge triggered Mono-Shot circuit, and converts to a valley detect (VD) signal. Furthermore the switching frequency of the proposed control scheme varies with the main inductance, input line voltage, and output power. The maximum switching frequency is limited for this application is 150 KHz (due to considerations of EMI standards). Both the VD signal and the maximum frequency signal F_{SMAX} are input to AND gate and then a SET signal is outputted to the SR flip-flop circuit, and to switch ON the Q_1 MOSFET at QR valley switching (Figure-17 and 18).

With v_{gs} going low indicates end of ON-time of MOSFET that triggers, the Mono-shot, of time fixed by 1nF and 716 Ohms, (Figure-18) a high pulse. This Mono-shot output switches ON the Transistor 2N7002, giving the comparator LM311 output low for the set-time. After that LM311 output is again high for next time when v_{gs} go low again. The qualified SET signal (i.e. logical AND of F_{SMAX} and VD) sets the SR Flip-Flop to high-state, so that the MOSFET is turned ON.

The turning OFF of the MOSFET is by v_{CS} getting compared with always V_{REF}, generating an output of error amplifier, which is acting as set-point for the comparator. This comparator has another input as COT-Ramp signal. When this V_{Ramp} is higher than error amplifier output, the RESETING of the SR flip-flop takes place, indicating end of ON-Time of MOSFET. For a fixed V_{LED}, with set constant current I_{LED} this ON-time is constant, and depends on setting of I_{LED} as $v_{CS} = I_{LED} R_{CS}$.

The Mode-I (Figure-14a) begins when Q_1 is switched ON, imposing V_{rec} on the inductor L. Since circuit operates on BCM or DCM; the inductor current i_L increases linearly from zero simultaneously, and rising slopes of i_L are proportional to the difference between V_{rec} and V_{LED}. The current i_L keeps increasing until Q_1 is switched OFF, at which instance the i_L reaches the peak value within the switching cycle. The peak value for inductor current i_L for a Constant-On-Time (for MOSFET) is depending on the V_{rec}; more the V_{rec}, higher is the $i_{L,peak}$.

The switching OFF of the MOSFET Q_1 marks the onset of Mode-II. During the Mode-II (Figure-14b) the current i_L declines from the peak continuously. The down slope of i_L depends on the output voltage V_{LED}, and for a constant V_{LED}, the un-slope remains constant always at what ever is value of V_{rec}. Moreover, the upslope depends on V_{LED} (constant) and the peak value i_L are proportional to the difference of V_{rec} and V_{LED}. Thus the duration that i_L declines to zero varies with input voltage V_{rec}, or say input voltage. More the input voltage V_{rec} more is the time for i_L to go to zero. That is discharge time t_{dis} as mentioned in the Figure-15. This we have discussed also in previous section. It means that the discharge time t_{dis} of i_L is varied, and thus the switching frequency may be varied with V_{rec}. Thus we may have higher switching frequency at lower V_{rec} and vice-versa. This mode ends when i_L is zero, and operation proceeds to Mode-III.

See the Figure-15a and b, drawn for high input voltage and low input voltage respectively; for Constant-On-Time (COT) case. For high input voltage V_{rec} the peak inductor current at end of Mode-I is higher in Figure-15a, with steeper up-slope as compared to Figure-15b where V_{rec} is low. The discharge phase Mode-II show that i_L down-slopes at same rate in both the cases, and for Figure-15b, the time i_L go to zero is smaller, i.e. t_{dis}. This is what we discussed in above paragraph. Now if we take the instance at which the current i_L go to zero-as next switch ON instance for BCM operation, then we find that we require higher switching frequency when input voltage is lower. We discuss the switching ON of MOSFET instance next-and later in some detail discussing QR valley switching.

At the start of Mode-III the inductor current i_L has declined to zero. The main inductance L and parasitic capacitance form a resonant tank. Figure-14c gives the equivalent circuit where the main inductor L resonates with C_f the EMI filter capacitor, drain-source capacitor C_{DS} and parasitic capacitance of the freewheeling diode C_{D0}, and the output capacitor C_0 . Figure-15 shows the waveforms. As per $L-C$ resonance the resonant inductance current is 90^0 leading to capacitor voltage. In other words the peak and valley of the of the resonant capacitance voltage are at zero crossings of the resonant inductor current (more clear in Figure-15b). Therefore the drain-source voltage V_{DS} resonates to its valley when inductor current i_L resonates to zero crossing at t_{dis} meaning the V_{DS} valley can be sensed when i_L reaches zero crossing consequently. Therefore QR valley detector senses the i_L (via v_{CS}) and compares with reference signal and when this sensed signal is lower then gives *VLY* signal (Figure-15). The gate driver outputs the v_{gs} signal to switch the MOSFET Q_1 and operation returns to Mode-I. We will discuss QR valley switching in later section. Also it may be noted that while input voltage is high, the circuit operates on BCM (almost), but at lower input voltage the circuit is operating on purely DCM.

Circuit Calculations

In order to derive expressions and apply for calculations, let us assume-a) Besides the parasitic capacitance of MOSFET and the freewheeling diode D_0 all the other components are ideal; b) The capacitance C_f is small and the EMI filter is eliminated; V_{rec} is a purely rectified sinusoid voltage source; c) the output capacitor C_0 is large enough so that V_{LED} can be regarded as constant DC voltage. The circuit is supplied by the line voltage source which is

$$v_{ac}(t) = V_m \sin\left(2\pi f_L t\right) \tag{44}$$

Where V_m and f_L are amplitude and frequency of the input voltage. The rectified voltage Is following

$$V_{\text{rec}}(t) = V_m \left|\sin\left(2\pi f_L t\right)\right| \tag{45}$$

Due to the fact that f_L (50 Hz) is much lower that the switching frequency f_S (100 KHz), V_{rec} can be considered as a constant. The buck converter has to obey following condition

$$V_{LED} \geq \left(V_{\text{rec}}(t)\right)\left(D\right) \tag{46}$$

Where V_{LED} and D are output voltage and duty ratio respectively. In expression (8) we stated $E_{dc} D \leq \left(N_1 / N_2\right) V_0 \left(1-D\right)$, here $N_1 / N_2 = 1$ $E_{dc} = V_{\text{rec}}(t)$ and $V_0 = V_{LED}$. Since the buck converter is only able to acquire the input power when the input voltage is higher than the output voltage. In other words the circuit can only follow the input current through the bridge rectifier when V_{rec} is higher than V_{LED}; the waveforms are given in Figure-16. As we see the current i_L increases from

zero once Q_1 is switched ON and the current reaches its peak at the end of Mode-I. It is noted that the line voltage source supplies the load (buck converter) only during Mode-II. The rectified input current i_{rec} is equal to i_L when Q_1 is switched ON, and the peak i_L are enveloped within a sinusoidal in phase with line input voltage when Q_1 is switched ON. The rising inductor current is

$$i_L(t) = \frac{|V_{\text{rec}}(t) - V_{LED}|}{L_m} t$$

This current is input current in Mode-I, i.e. $i_{in}(t) = i_L(t)$ for $0 < t < DT_S$. The peak currents of i_L and i_{rec} are following, takes place at $t = DT_S$

$$i_{L,peak}(t) = \frac{|V_{\text{rec}}(t) - V_{LED}|}{L}(DT_S) = \frac{|V_{\text{rec}}(t) - V_{LED}|}{(L)(f_S)} D \tag{47}$$

In the Mode-II when MOSFET is OFF, the inductor current though decays in the time interval $DT_S < t < T_S$, but the input current from source is zero, i.e. $i_{in}(t) = 0$. The average input current $i_{in}(t)$ can be written as following (as same was derived in previous section)

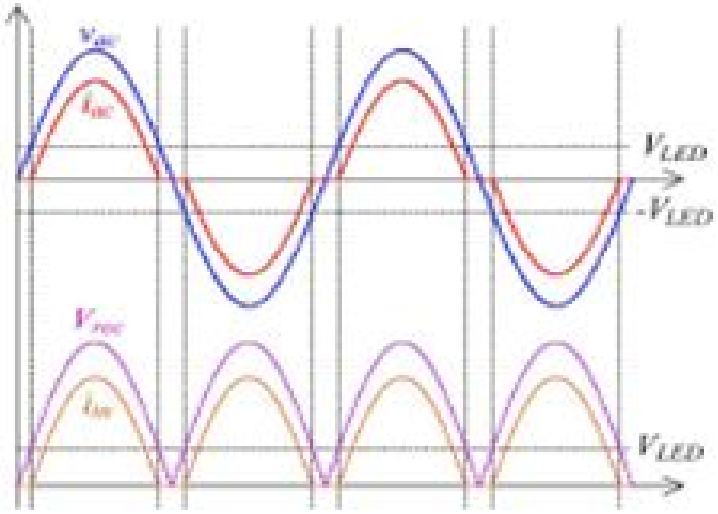


Figure-16: Theoretical input waveforms of voltage and current

$$i_{in,avg}(t)=\frac{1}{T_S}\int_0^{T_S} i_{in}(t)\mathrm{d}t \qquad i_{in}(t)=i_L(t)=\frac{\left|V_{\mathrm{rec}}(t)-V_{LED}\right|}{L}t, \quad 0<t<DT_S$$

$$i_{in}(t)=0, \qquad DT_S<t<T_S$$

$$i_{in,avg}(t)=\frac{1}{T_S}\int_0^{DT_S}\frac{\left|V_{\mathrm{rec}}(t)-V_{LED}\right|}{L}\bar{t}\,\mathrm{d}\bar{t}+\frac{1}{T_S}\int_{DT_S}^{T_S}\left(i_{in}(\bar{t})=0\right)\mathrm{d}\bar{t}$$

$$=\frac{1}{T_S}\left[\frac{\left|V_{\mathrm{rec}}(t)-V_{LED}\right|}{L}\left(\frac{\bar{t}^2}{2}\right)\right]_0^{DT_S}=\frac{\left|V_{\mathrm{rec}}(t)-V_{LED}\right|}{2L}D^2T_S$$

$$=\frac{\left|V_{\mathrm{rec}}(t)-V_{LED}\right|}{2L\ f_S}D^2=\frac{i_{L,peak}}{2}D; \qquad i_{L,peak}=\frac{\left|V_{\mathrm{rec}}(t)-V_{LED}\right|}{(L)(f_S)}D$$

$$i_{in,avg}(t)=\frac{i_{L,peak}(t)}{2}(D)$$

$$=\frac{\left|V_{\mathrm{rec}}(t)-V_{LED}\right|}{2(L)(f_S)}(D^2) \tag{48}$$

$$=\frac{\left|V_{\mathrm{rec}}(t)-V_{LED}\right|}{R_{in}}; \qquad R_{in}=\frac{2L\ f_S}{D^2}$$

R_{in} is equivalent resistance of the buck-converter given as

$$R_{in}=\frac{2L\ f_S}{D^2} \tag{49}$$

According to Figure-16, and (47) and (48); the input current can be expressed as

$$i_{in}(\theta)=I_m\left(\sin\theta-\sin\theta_1\right) \tag{50}$$

Where I_m and θ_1 are maximum input current and conduction angle respectively, that is

$$I_m=\left.\frac{\left|V_{\mathrm{rec}}(t)-V_{LED}\right|(D)^2}{2(L)(f_S)}\right|_{\max} \tag{51}$$

$$\theta_1=\sin^{-1}\left(\frac{V_{LED}}{V_m}\right) \tag{52}$$

Average input power of the driver circuit P_{in} can be obtained from following expression

$$P_{in}=\frac{P_{LED}}{\eta}=\frac{V_mI_m}{\pi}\int_{\theta_1}^{\pi-\theta_1}\left(\sin^2\theta-\sin\theta\sin\theta_1\right)\mathrm{d}\theta$$

$$=\frac{V_m\left(V_m-V_{LED}\right)(D)^2}{4(L)(f_S)}\left(1-\frac{2\theta_1}{\pi}-\frac{\sin 2\theta_1}{\pi}\right) \tag{53}$$

Where P_{LED} and η are the output power and the system efficiency respectively. The buck-converter inductance can be designed as per the formula obtained from (53) as

$$L=\frac{\eta\,V_m\left(V_m-V_{LED}\right)(D)^2}{4P_{LED}f_S}\left(1-\frac{2\theta_1}{\pi}-\frac{\sin 2\theta_1}{\pi}\right) \tag{54}$$

The duty ratio is given as

$$D = \sqrt{\frac{4P_{LED}L\ f_S}{\eta\, V_m\left(V_m - V_{LED}\right)\left(1-\frac{2\theta_1}{\pi}-\frac{\sin 2\theta_1}{\pi}\right)}} \tag{55}$$

Moreover C_0 is determined by following formula

$$C_0 = \frac{\sqrt{\left(\frac{2I_{LED}}{\Delta I_{LED}}\right)^2 - 1}}{4\pi f_L R_D} \tag{56}$$

Where I_{LED} and ΔI_{LED} are average and ripple values of output current respectively and R_D is total dynamic resistance of LED. The derivation of (56) is with ΔI_{LED} taken as deviation of LED current from set value I_{LED}, we will have minimum current as $I_{LED-\min} = I_{LED} - \frac{\Delta I_{LED}}{2}$ and maximum current $I_{LED-\max} = I_{LED} + \frac{\Delta I_{LED}}{2}$. The geometric mean of the fluctuating current is $\langle I_{LED}\rangle_{\mathrm{GM}} = \sqrt{\left(I_{LED-\min}\right)\left(I_{LED-\max}\right)}$. We get

$$\begin{aligned}\langle I_{LED}\rangle_{\mathrm{GM}} &= \sqrt{\left(I_{LED} - \frac{\Delta I_{LED}}{2}\right)\left(I_{LED} + \frac{\Delta I_{LED}}{2}\right)} \\ &= \sqrt{\left(I_{LED}\right)^2 - \left(\frac{\Delta I_{LED}}{2}\right)^2}\end{aligned}$$

The capacitor C_0 needs to pump in charge of $\langle q\rangle = \left(\langle I_{LED}\rangle_{GM}\right)\left(T_L\right)$ to the load in line-cycle time period T_L; where $\frac{1}{T_L} = 2\pi f_L$; with f_L as line frequency of 50Hz. The charge lost in the capacitor C_0 in the same time-period is $C_0\left(\Delta V_{LED}\right)$; we can write $\Delta V_{LED} = R_D\left(\Delta I_{LED}\right)$. Thus charge balance gives the following

$$\begin{aligned}C_0\left(\Delta V_{LED}\right) &= \left(\langle I_{LED}\rangle_{\mathrm{GM}}\right)\left(T_L\right) \\ C_0 R_D\left(\Delta I_{LED}\right) &= \left(\sqrt{\left(I_{LED}\right)^2 - \left(\frac{\Delta I_{LED}}{2}\right)^2}\right)\left(T_L\right) \\ C_0 &= \frac{\sqrt{\left(I_{LED}\right)^2 - \left(\frac{\Delta I_{LED}}{2}\right)^2}}{2\pi f_L R_D\left(\Delta I_{LED}\right)} = \frac{\left(\frac{\Delta I_{LED}}{2}\right)\sqrt{\left(\frac{I_{LED}}{\Delta I_{LED}/2}\right)^2 - 1}}{2\pi f_L R_D\left(\Delta I_{LED}\right)} \\ &= \frac{\sqrt{\left(\frac{2I_{LED}}{\Delta I_{LED}}\right)^2 - 1}}{4\pi f_L R_D}\end{aligned}$$

So we have derived (56) by charge balance. Now we see why we have taken Geometric Mean of the ripple current. Take a case that ΔI_{LED} we want to make small to $\pm 25\%$ from say $\pm 50\%$ for a constant I_{LED} (say 200mA). If we take normal arithmetic mean (AM) then irrespective of ΔI_{LED} requirement, we need to pump in always same amount of coulombs from C_0; as $\langle I_{LED}\rangle_{\mathrm{AM}} = I_{LED}$. The geometric mean says for larger ΔI_{LED}, the

$\langle I_{LED} \rangle_{\text{GM}}$ requirement is lesser needs lesser coulombs. Therefore GM gives a reality better in this case id AM is taken. However with AM instead of GM, we will arrive at

$$C_0 = \frac{\left(\frac{I_{LED}}{\Delta I_{LED}}\right)}{2\pi f_L R_D}$$

We will use (56) in our calculations of finding C_0.

Let us derive the values with input voltage v_{ac} RMS as (85V_{RMS} to 265V_{RMS}). We put a constraint on maximum duty ratio $D_{\max} = 45\%$. We assume $\eta = 90\%$. We have LED system with $V_{LED} = 40\text{V}$ comprising of 12 LEDs in series with $I_{LED} = 200\text{mA}$ and ripple $\Delta I_{LED} = \pm 25\%$. The dynamic resistance is $R_D = 2\Omega$ per LED. The $P_{LED} = (40\text{V})(0.2\text{A}) = 8\text{W}$; and let us have minimum switching frequency $f_{S,\min} = 50\text{kHz}$, maximum switching frequency as $f_{S,\max} = 150\text{kHz}$. The maximum conduction angle $\theta_{1-\max}$ is following for $V_{m,\min} = \sqrt{2}V_{in-\text{RMS},\min}$ that is $\sqrt{2}(85\text{V}) = 120\text{V}$ is

$$\theta_{1,\max} = \sin^{-1}\left(\frac{V_{LED}}{V_{m,\min}}\right) = \sin^{-1}\left(\frac{40}{\sqrt{2}(85)}\right) = 19.436^0 \tag{57}$$

For minimum switching frequency $f_{S,\min} = 50\text{kHz}$ and minimum $V_{m,\min} = 120\text{V}$, we have L with (57) as

$$\begin{aligned} L &= \frac{\eta V_{m-\min}\left(V_{m-\min} - V_{LED}\right)\left(D_{\max}\right)^2}{4P_{LED} f_{S-\min}}\left(1 - \frac{2\theta_{1-\max}}{\pi} - \frac{\sin 2\theta_{1-\max}}{\pi}\right) \\ &= \frac{0.9\times 120\times(120-40)\times 0.45^2}{4\times(40\times 0.2)\times\left(50\times 10^3\right)}\left(1 - \frac{2\times(19.436^0)}{180^0} - \frac{\sin\left(2\times(19.436^0)\right)}{180^0}\right) \\ &= 853.5\mu\text{H} \end{aligned} \tag{58}$$

Let us work with $L = 820\mu\text{H}$; with this we get the maximum duty ratio $D_{\max}$ (re-calculated) as following

$$\begin{aligned} D_{\max} &= \sqrt{\frac{4P_{LED}L\ f_{S-\min}}{\eta V_{m-\min}\left(V_{m-\min} - V_{LED}\right)\left(1 - \frac{2\theta_{1-\max}}{\pi} - \frac{\sin 2\theta_{1-\max}}{\pi}\right)}} \\ &= \sqrt{\frac{4(40\text{V}\times 0.2\text{A})(820\times 10^{-6})(50\times 10^3)}{(0.9)\ (120\text{V})(120\text{V} - 40\text{V})\left(1 - \frac{2\times 19.436^0}{180^0} - \frac{\sin(2\times 19.436)}{180^0}\right)}} \\ &= 41.11\% \end{aligned} \tag{59}$$

The ΔI_{LED} ripple current $\pm 25\%$ means $\Delta I_{LED} = 2\left(\frac{25}{100}\right)\left(I_{LED}\right) = 0.5\times(0.2\text{A}) = 0.1\text{A}$, with total dynamic resistance as $R_D = 12\times\left(2\Omega\right) = 24\Omega$, with $f_L = 50\text{Hz}$, we obtain C_0 by (56) as

$$C_0 = \frac{\sqrt{\left(\frac{2I_{LED}}{\Delta I_{LED}}\right)^2 - 1}}{4\pi f_L R_D}$$

$$= \frac{\sqrt{\left(\frac{2\times(0.2\text{A})}{0.5\times(0.2\text{A})}\right)^2 - 1}}{4\times\pi\times 50\times(12\times 2\Omega)} = \frac{\sqrt{15}}{4\times\pi\times 50\times(12\times 2\Omega)} \tag{60}$$

$$= 257\,\mu\text{F}$$

The maximum ratings for Q_1 and D_0 is following

$$V_{Q_1-\max} = V_{D_0-\max} = V_{m-\max} = \sqrt{2}\times 265\text{V} = 374.77\text{V} \tag{61}$$

$$I_{Q_1-\max} = I_{D_0-\max} = \frac{\left(V_{m-\min} - V_{LED}\right)\left(D_{\max}\right)}{L\ f_{S-\min}}$$

$$= \frac{(120\text{V} - 40\text{V})\times 0.45}{\left(820\times 10^{-6}\right)\times\left(50\times 10^{3}\right)} = 0.878\text{A} \tag{62}$$

The duty ratio is maximum when input voltage is minimum, for maintaining constant V_{LED} , see (46) i.e. $V_{LED} \geq \left(V_{\text{rec}}(t)\right)\left(D\right)$ and (55); that is what is used in (62)

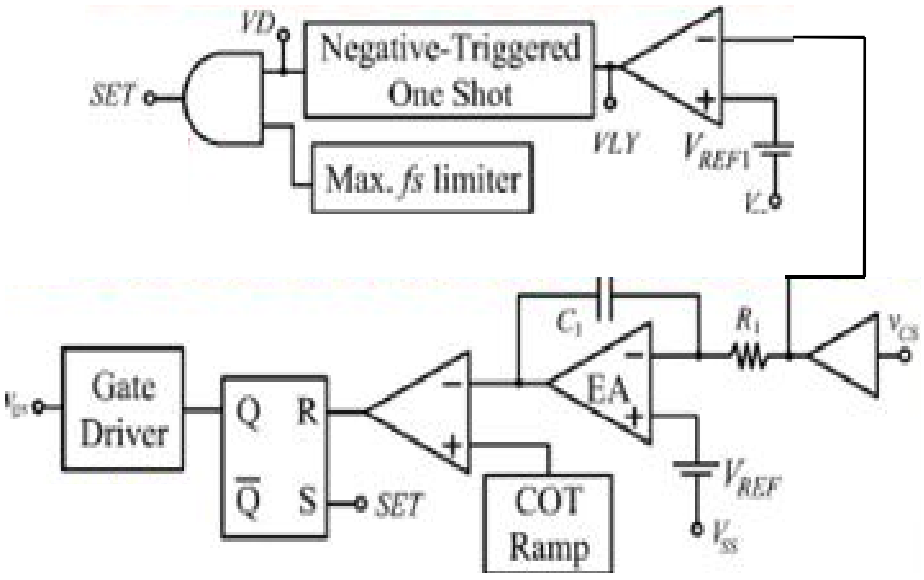


Figure-17: QR Valley Detection and Switching Control Scheme

To implement the output current regulation, the current sense resistance R_{CS} (Figure-13) should be designed. In this circuit scheme (Figure-18), amplifier gain is $K = 6$, and this

amplified voltage v_{CS_6X} is being compared with V_{REF}; which is 1.2V, i.e. from circuit of Figure-19, we get V_{REF} as $\frac{60\text{k}\Omega}{60\text{k}\Omega+190\text{k}\Omega}(5\text{V})=1.2\text{V}$; gain as $K=6$. Therefore we have $K(v_{CS})=V_{REF}$; and $v_{CS}=I_{LED}R_{CS}$; which gives

$$R_{CS}=\frac{1.2\text{V}}{6\times 0.2\text{A}}=1\Omega \tag{63}$$

Moreover R_{CS} is in series with L and conducts major current, the power rating of R_{CS} is dissipation in R_{CS} given by following

$$P_{R_{CS}}=I_{LED}^2R_{CS}=(0.2\text{A})^2\times 1\Omega=40\text{mW} \tag{64}$$

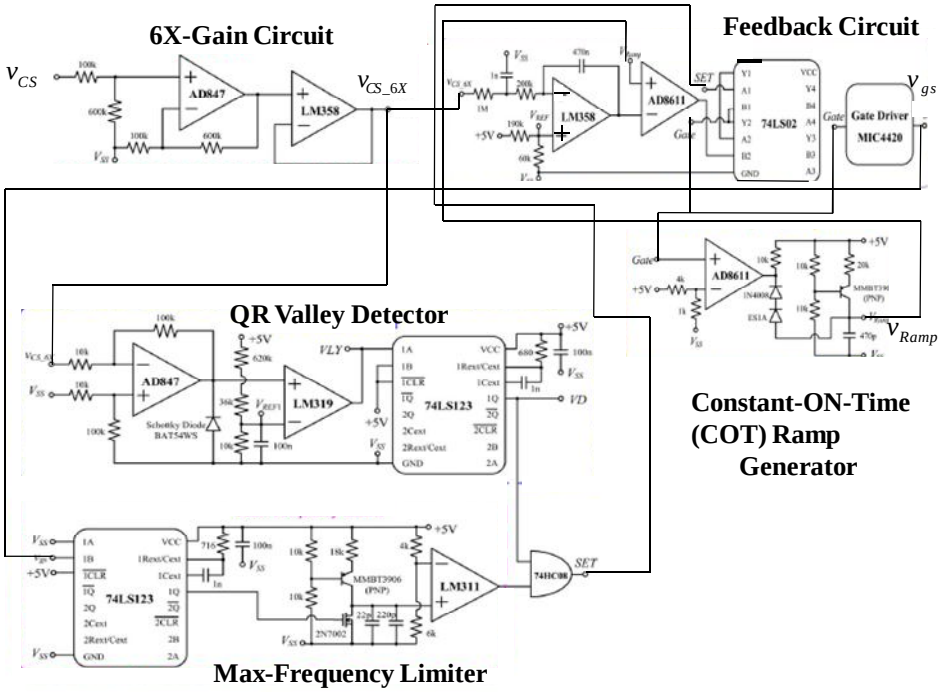


Figure-18: Control circuit for QR valley switching

For EMI filtering $L_f=4\text{mH}$ and $C_f=0.1\mu\text{F}$ will do, to filter out high frequency contents. The circuits in Figure-18 are powered with 5V respect to V_{SS} point (floating ground).

We see the circuit of Figure-18 COT Ramp Generator Circuit. We see that $100\mu\text{A}$ constant current charges a 470nF capacitor, when Gate signal is high (i.e. at the start of ON period of MOSFET. The 470pF capacitor is kept otherwise discharged at V_{Ramp} of about 1V (two diodes 1N4008 and ES1A are forward biased when AD8611 comparator output is low when Gate signal is zero during OFF period). Thus to charge the 470pF capacitor from say 1V to 5V the time period is about $20\mu\text{s}$. Thus we see that ramping up of the V_{Ramp} starts at start of ON period of MOSFET. The resetting of this COT-Ramp takes place at the point when Gate-signal goes low indicating end of ON-period; and it happens well before the V_{Ramp} reaching 5V. This COT-Ramp signal is used

for re-setting the SR Flip-flop by comparing with error amplifier (comparator) output (Figure 17 & 18).

The error amplifier compares v_{CS_6X} signal to 1.2V as shown in (63). The average DC value of v_{CS_6X} is 1.2V, but actually this reflects the inductor current, i_L which is triangular wave, going up and down from zero to $v_{CS\_6X-\max}$. Therefore instantaneously this voltage goes more than 1.2V and also less than 1.2V periodically-and thus making the Error-Amplifier LM358 ramp up and ramp low around average value governed by $RC\frac{dv_{0-E/A}(t)}{dt} = 1.2\text{V} - v_{CS\_6X}(t)$. The output voltage of error amplifier is $v_{0-E/A}$; that is integral action given as $v_{0-E/A}(t) = \frac{1}{RC}\int_0^t \left(1.2\text{V} - v_{CS\_6X}(\bar{t})\right)d\bar{t} + v_{0-avg}$; where v_{0-avg} is initial voltage i.e. $v_{0-E/A}(0)$ and is a constant value. Refer Figure-18 $R = 1.2\text{M}\Omega$ and $C = 470\text{nF}$, we get from error amplifier circuit. We see that the average value of the amplifier LM358 output is about 2.5V maximum-(if we assume 50% duty cycle of the square wave output of the Error Amplifier LM358-by removing feed-back capacitor). This voltage is the set-point for the V_{Ramp} signal. This when the V_{Ramp} signal rising from 1V towards 5V crosses this set-point; we will get high signal at the output of comparator LM8611 indicating end of ON-period, asking RESETTING of SR flip-flop.

Quasi Resonant Mode Operation & Valley Switching Fundamentals

A Quasi-Resonant fly-back is a simple DCM fly-back having a valley switching turn-ON mechanism. It is also known as variable frequency or valley switching fly-back and largely suited for low power SMPS applications as charger, adapter, LED and auxiliary supply. Quasi-resonant conversion works in a quite different way than the well known resonant converters. Figure-19a shows the basic circuit and drain-source voltage waveform of primary MOSFET switch in a fly-back converter, operating in DCM. During the first time interval (Mode-I) the drain current ramps up until the desired peak current is reached. The MOSFET then turns OFF. The leakage inductance L_{leak} in the fly-back transformer rings with the MOSFET parasitic capacitance C_{eqp} and causes a high voltage spike, which is limited by snubber clamp circuit. After this inductive spike has damped, the drain voltage equals the input voltage plus the reflected output voltage.

The drain voltage would immediately drop to the bus voltage when the current in the output diode drops to zero, if the parasitic ring of the primary inductance and parasitic capacitance are ignored. However, the drain voltage rings down to level as shown in Figure-19a and 19b, due to parasitic resonance by the primary inductance L_m or say L_p and parasitic capacitance C_{eqp} or CD. For example the inductance 1mH and the parasitic capacitance is 100pF, and then the resonance frequency is 500 kHz. The resonant circuit is lightly damped and the resonance frequency is given below is independent of the input voltage and load current.

$$f_{resonant} = \frac{1}{2\pi\sqrt{L_m C_{eqp}}} \tag{65}$$

Where L_m (or L_p) is the primary inductance; C_{eqp} is the equivalent primary side parasitic capacitance which including parasitic capacitance of the primary winding, the parasitic MOSFET and the parasitic capacitance of the secondary side (including secondary winding and output rectifier diode) reflect to primary side i.e. *CD* on drain node.

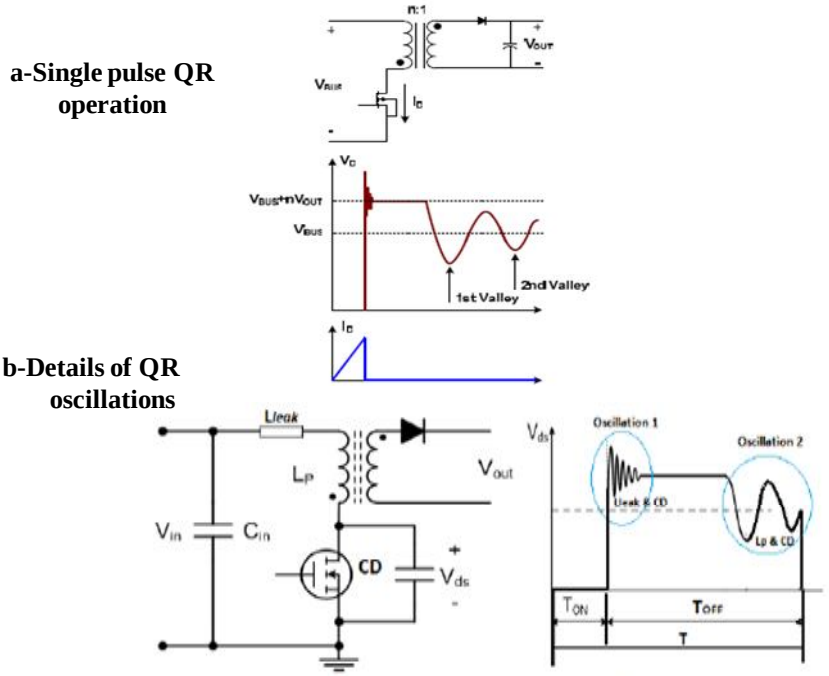


Figure-19: Single pulse of Fly-Back Converter showing Quasi Resonance Oscillations

Figure 19b circuit show in details the primary parasitic components the L_{leak}, the leakage inductance and total Drain-Source Capacitance *CD* (including intra-winding capacitance and stray capacitance etc). Figure-19b also showing timing diagram that shows the wave-form of the V_{ds} in detail, where two oscillations are shown. The higher frequency oscillation-1 happens during the initial turn-OFF of the MOSFET due to leakage inductance resonating with CD and the oscillation-2 happens when secondary winding energy reduces to zero. During this time both windings are open, thus L_p (or L_m) resonate with capacitance at CD node.

In a conventional fixed-frequency fly-back converter at DCM operation, the MOSFET (at primary side); is turned ON at a fixed frequency and turned OFF when the current reaches the desired level. The device (MOSFET) turn-ON time (i.e. end of Mode-II) may occur at any point during parasitic resonance. In some cases the device may turn ON when the drain voltage is lower than the bus voltage (means low switching loss and thus high efficiency); and in some cases the switch will turn ON when the drain voltage is higher than bus voltage (implies high switching loss). This characteristic is often

observed on the efficiency curves of DCM operated converters with constant load, the efficiency fluctuated with the input voltage as the turn-ON switching loss changes due to the variation of the drain voltage at the MOSFET turn-ON point.

In Quasi-Resonant (QR) operation, the switch does not have a fixed switching frequency. Instead switch will turn ON by the controller (as described in Figure-17 and 18), when the drain voltage reaches its minimum value (valley point; refer Figure-20). The time period say T_W is half the resonant period determined by the transformer magnetization inductance and parasitic capacitance. The switch ON time T_1 is small as less energy is determined by output feed back loop as conventional peak current mode control. For light load condition the time T_1 is small as less energy is required by the load, resulting in small peak current, and also a shorter output diode conduction time. Therefore switching frequency increases in QR fly-back operation as load decreases, which may deteriorate the light load efficiency and challenges the EMI limits. In order to eliminate these problems a frequency clamp function (Figure-17 and 18) is added into the controller to limit the maximum switching frequency (150 K Hz).

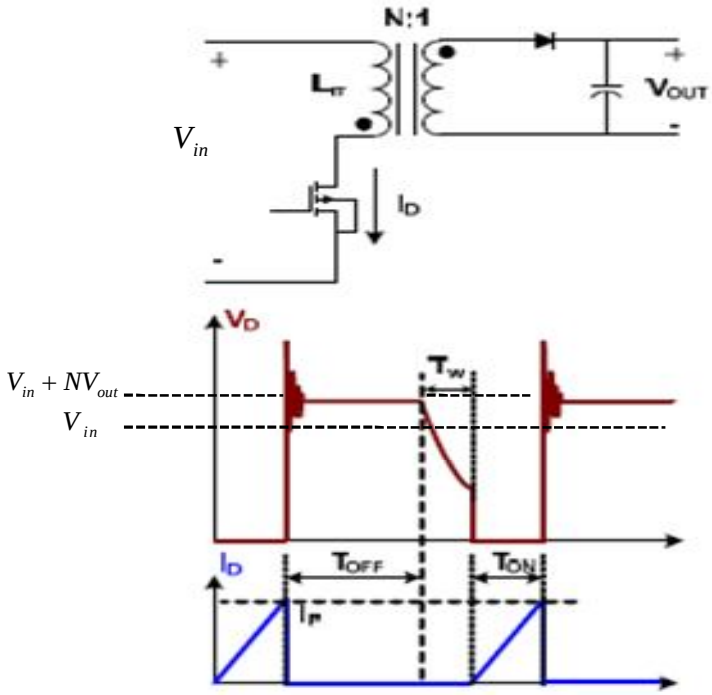


Figure-20: QR Valley Switching

Compared to the traditional fly-back under CCM and DCM operation, the QR operation can minimize the turn-ON switching loss of the switch by switching at the valley point, thus increasing efficiency and lowering MOSFET temperature rise. Its main disadvantage that of higher switching frequency at light load is eliminated by the frequency clamp function in controllers, also by switching at low voltage and currents the EMI generated by QR operation is relatively low.

We recall the concept of L-C resonance and recalling that we understand that at the instant when the secondary current of the transformer while free-wheeling and decaying

linearly from peak value (i.e. at the end of T_{ON}), goes to zero at the end of T_{OFF}, the resonance starts; (refer Figure-20). The resonance or oscillation starts at the end of T_{OFF}; and L-C resonance says that the capacitor voltage lags the inductor current (while resonating) by 90^0. Thus zero crossing of the secondary current (this is magnetization primary current too); leads the falling Drain-Source voltage. We see a delay of time T_W at which the voltage goes to minimum value after current has gone to its minimum value- due to this phase difference concept. Thus peaks and valley of the voltage and currents are having this phase (time) difference. This we had discussed in previous section briefly.

The primary inductance L_m and peak current I_p determines the power can be transferred to output side (7) i.e.

$$P_{in} = \frac{1}{2} L_m I_p^2 f_S = \frac{P_{out}}{\eta} \tag{66}$$

We can have circuit efficiency as η estimated to be 0.8-0.9. The Figure-20 shows the primary side MOSFET Drain-Source voltage and current in QR fly-back converter. It is preferred that the primary switch turns ON at the first valley at heavy load condition to minimize the peak current. Each period can be calculated as

$$T_{ON} = \frac{L_m I_p}{V_{in}} \tag{67}$$

$$T_{OFF} = \frac{L_m I_p}{N V_{out}} \tag{68}$$

$$T_W = \pi \sqrt{L_m C_{eqp}} \tag{69}$$

From (67), (68) and (69) we have switching frequency as

$$f_S = \frac{1}{T_{ON} + T_{OFF} + T_W} \tag{70}$$

Using (66) and (67)-(70) we write

$$\frac{P_{out}}{\eta} = \frac{1}{2} L_m I_p^2 \left(\frac{1}{\frac{L_m I_p}{V_{in}} + \frac{L_m I_p}{N V_{out}} + \pi \sqrt{L_m C_{eqp}}} \right) \tag{71}$$

Neglecting the T_W, which is small compared to T_{ON} and T_{OFF} we get

$$\frac{P_{out}}{\eta} = \frac{1}{2} L_m I_p^2 \left(\frac{1}{\frac{L_m I_p}{V_{in}} + \frac{L_m I_p}{N V_{out}}} \right) \tag{72}$$

From (72) we get

$$I_p = \frac{2 P_{out}}{\eta} \left(\frac{1}{V_{in}} + \frac{1}{N V_{out}} \right) \tag{73}$$

From above we obtain max peak current I_p at minimum line voltage $V_{in-\min}$;

$$I_{p-(V_{in-\min})} = I_{p-\max} = \frac{2 P_{out}}{\eta} \left(\frac{1}{V_{in-\min}} + \frac{1}{N V_{out}} \right)$$

and from that we calculate L_m as.

$$L_m = \frac{2P_{out}}{\eta}\left(\frac{1}{I^2_{p-(V_{in-\min})} f_{S-\min}}\right) \quad (74)$$

Where $f_{S-\min}$ is the expected minimum switching frequency at lowest line voltage at fully loaded condition.

Valley Switching Detection via Sensing the Voltage across inductor

After discussing the fundamentals of fly-back converter and QR valley switching concepts; let us see how simply we can detect the valley point, and then use the same to switch ON the MOSFET. Out of the several simple fly-back circuits discussed, we take the circuit of Figure-12. In earlier discussion we used the v_{CS}, to detect i_L and used this valley switching schemes-as mentioned in Figure-17 and 18.

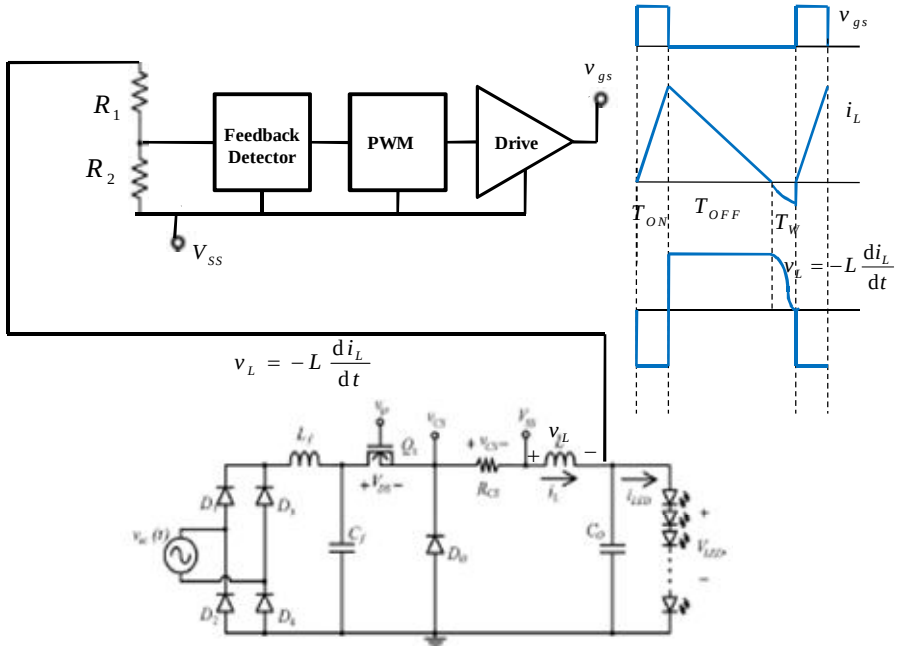


Figure-21: QR Valley switching from inductor voltage sensing

In stead if we tap the inductor voltage as shown in Figure-21, i.e. v_L, use voltage division, by resistors, and use to detect valley of i_L; that is point when $v_L = -L\frac{di_L}{dt}$ goes to zero, as the instance of turn ON of the MOSFET, gives simpler circuit scheme. However, the $v_{CS} = i_L R_{CS}$ is still to use to set LED current by comparing this in error amplifier with reference voltage as $I_{LED} = \left(V_{REF} / R_{CS}\right)/K$. In the scheme presented above we see that T_{ON} and T_W are constants, but T_{OFF} decreases with input voltage. We can have say 10μs as minimum value of $T_S = T_{ON} + T_{OFF} + T_W$; for minimum input voltage of say 90V. The

circuit of Figure-1 always switches at first valley detect. The other switching control scheme remains the same as in Figure-17 and 18.

Conclusions

A simple electronics to drive a LED bulb has thrown several concepts related to power electronics. We have discussed the basics of fly-back converter, especially single stage power factor correction circuits to drive LED lamps for lighting applications. We have discussed and derived basic equations required for understanding the concepts. The fly-back converter is operated in discontinuous conduction mode and at constant frequency providing and input power factor high enough to satisfy the power input quality standards. The first topology is discussed with transformer isolated fly-back converter. After that we developed the non-isolated fly-back converter requiring single energy store inductor. A novel Quasi-Resonant (QR) Valley switching scheme for getting high power factor and higher circuit efficiency is also discussed. This topology is the most modern technique, requires low component count (mainly requires only one energy store inductor, instead of a transformer), and achieves greater efficiency-by using QR Valley switching of MOSFET. This note also discusses the detection of valley switching instance by sensing inductor current via use of sense resistor; also via the use of inductor voltage-and thus avoids the use of auxiliary winding schemes. Thus we conclude that a simple application to drive LED lamps; is not too simple as one may think; requires lot of concepts of power electronics and that we presented. Whatever schemes we discussed for low power LED drives, get integrated ON-Chip solutions-with only the freewheel diode, output capacitor, storage inductor, sense resistors EMI filter and bridge rectifier, plus few extra resistors and capacitors need be placed externally. Though ON-Chip solutions are available, the basic understanding is however required and need to be developed for better understanding and further improvements.

References

J.J. Sammarco, M. A. Reyes, J. R. Bartels, Sean Gollagher, “Evaluation of peripheral visual performace when using incandescent and LED Miner lamps”, IEEE Transactions on Industry Applications; Vol. 45; No. 6, pp1923-1929, Nov/Dec 1999.

John. L. Giuliani, George M. Petrov, Robert E. Pechacek, Robert A Mager, “Plasma study of a Moly-Oxide-Argon-Discharge-Bulb”, IEEE Transactions on Plasma Science, Vol 31, No. 4, pp564-571, August 2003.

J Cunill-Sola, M J Salichs, “Study and Characterization of Waveforms from Low Watt (< 25W) Compact Fluorescent Lamps with Electronic Ballasts”, IEEE Transactions on Power Delivery; Vol. 22. No. 4, pp2305-2311, October 2007.

Y C Chuang, C S Moo, H W Chen, T F Lin, “A novel single stage High Power Factor Electronic Ballast with Boost Topology for Multiple Fluorescent Lamps, IEEE Transactions on Industry Applications”, Vol. 45, No. 1, pp323-331; Jan/Feb 2009.

M Rico-Secades, A J Calleja, J Ribas, E. L. Corominas, J M Alonso, J, Cardesin, J Garcia-Garcia, “Evaluation of low cost Permanent Emergency Lighting System Based on High Efficiency LEDs” IEEE Transactions on Industry Applications, Vol. 41, No.5 pp1386-1390, Sept/Oct 2005.

Y Jang, D L Dillman, M M Jovanovic, “A new soft-switched PFC Boost Rectifier with integrated Fly-Back Converter for Standby Power,” IEEE Transaction on Power Electronics, Vol. 21, No.1, pp66-72 Jan 2006.

R T Chen, Y Y Chen, “Single stage push pull boost converter with integrated magnetic and input current shaping technique”, IEEE Transaction on power electronics, Vol. 21, No.5, pp1193-1203, Sept-2006.

J Sun, M Chen, K J Karimi, “ Aircraft Power System Harmonics involving single-phase PFC converters”, IEEE Aerospace and Electronics Systems Vol.24, No.1, pp217-226 Jan-2008.

D G Lamar et al, “Design oriented analysis and performance evaluation of a low cost high brightness LED driver based on fly-back power factor corrector”, IEEE Transactions on Industrial Electronics, Vol. 60, No. 7, pp2614-2626, Jun-2013.

Y. C. Li, C L Chen, “A novel single stage high power factor ac-to-dc LED Driving circuit with leakage inductance energy recycling”, IEEE Transactions on Industrial Electronics, Vol. 59, No. 2 pp793-802, Feb 2012.

Y C Li, C L Chen, “ A novel primary side regulation scheme for single stage high power factor ac-dc-LED driving circuit”, IEEE Transactions on Industrial Electronics, Vol. 60, No. 11, pp4978-4986 Nov-2013.

“Single stage Buck and PFC Controller for LED lighting”, Silergy Corporation CA USA Application Note-2011.

J M Alonso, J Vina, D Gacio, G Martinez, R O Sanchez, “Analysis and design of the integrated double buck-boost converter as high power factor driver for power LED lamps”, IEEE Transactions on Industrial Electronics, Vol. 59, No. 4, pp1689-1697, April-2012.

H L Cheng, C W Lin, “Design and implementation of a high power factor LED driver with zero voltage switching on characteristics”, IEEE Trans. On Power Electronics Vol. 29, No. 9, pp 4949-4958, 2014.

H Ma, et al, “ A novel valley-fill SEPIC-derived power supply without electrolytic capacitors for LED lighting applications”, IEEE Transactions on Power Electronics, Vol. 27, No. 6, pp3057-3071 June 2012.