Note on Harmonic Distortion Control & Power Factor Correction Circuitry for Switched Mode Power Supply (M+N)

Shantanu Das
Reactor Control Systems Design Section E & I Group B.A.R.C. Mumbai
Email: shantanu@barc.gov.in

December-2016

Abstract

At a time when lean manufacturing has become the mantra of industry, minimizing energy costs has assumed ever greater importance. It's not just a matter of controlling consumption, however, but of how that consumption is billed by the utility. This is where power factor plays a key role. Power factor is the ratio of real power to apparent power in an electrical system. The lower the power factor, the higher the current draw. Higher current requires thicker wires and a more robust infrastructure in order to minimize power dissipation. Because this increases cost to utilities, facilities with low power factors get charged a higher rate. Fortunately, techniques exist to correct power factor and harmonics. In this note, we'll take a closer look at these concepts as they apply to servo motors and drives and various switch mode power supplies too. Power factor provides a measure of the efficiency of an electrical system. We are all familiar with power factor, but are we using it to its true potential? In this note we investigate the effect of harmonics on power factor and show why it is important to use 'true' power factor rather than classical 50Hz 'displacement' power factor, when describing non-linear loads. True power factor consists of two terms: displacement power factor and total harmonic distortion. It is frequently simplified to just displacement power factor, but that only holds for a specific class of linear loads. Servo drives and variable-frequency drives, Switch Mode Power Supplies etc. are nonlinear loads, so the classical simplification no longer applies. Thus increasing use of non-linear loads as electronic devices, as Switched Mode Power Supplies (SMPS) in Control & Instrumentation System has greatly increased the electrical stresses caused by harmonic currents on alternating-current power distribution networks. To maintain the quality of these networks, European Standard EN 60555-2 was created to set levels for harmonic currents injected by loads back on to the distribution network. There has however been much discussion about equipment classes and limits to apply to electronic equipment in general and equipment power supplies in particular. EN 60555-2 has recently been superseded by IEC 61000-3-2 which sets some more practical rules and provides a clearer definition of equipment classes. Thus we have spend efforts to control the input power quality of equipment power supply by enhancing power-factor (PF) close to unity and controlling the Total Harmonic Distortion (THD); to reduce the harmonic contents of the input current. In the latest embodiment of Fault Tolerant Power Distribution System (FTPDS) product marked as ECPS^{TM} (Electronics Corporation Power Supply) developed for NPCIL (PHWR700MW plant) we carried out Power Quality Tests as per IEC 61000-3-2; for PF and THD limits, as per IEC 61000-3-2 standards. The circuit employed for AC-DC ECPS for meeting this standard, is based on Active Power Factor Correction Circuitry–which reduces the Harmonic Contents of Input Current. In this note we will describe the working of the employed circuit.

Keywords: Displacement Power factor, Distortion Power Factor, True Power Factor, Total Harmonic Distortion, Boost–Converters, Duty Modulation, Continuous Conduction Mode, Active Power Factor Correction (PFC).

Introduction

From Electrical theory the concept of power factor used to be fairly simple to understand. However with the introduction of harmonics generated by today's non-linear loads, power factor analysis has become increasing complex which has contributed many power factor misconceptions. Power factor is a measure of how effectively a specific load consumes electricity to produce work. The higher the power factor, the more work produced for a given voltage and current. Power factor is always measured as ratio between real power in Watts (W) and apparent power in Volt-Ampere (VA). For linear loads which are defined as resistive inductive or capacitive, the apparent power in VA i.e. $S = V \times I$ is the vector sum of the reactive power Q in VAR and real power P in Watts. The power factor is $P / S = \cos\theta$, where θ the angle between S and P. This angle is the same as displacement angle between voltage and current for linear loads and therefore termed as Displacement Power Factor. For a given amount of current, increasing the displacement angle will increase Q, decrease P and lower the power factor. Purely resistive loads draw their currents in phase with the voltage and have a power factor of one. When the load is reactive it stores energy, releasing it during a different part of the cycle. Inductive loads such as electric motors cause their current to lag voltage, while capacitors cause their current to lead the voltage. Therefore lagging versus leading describes whether the net reactance is either inductive or capacitive.

The non-linear loads such as rectifier circuits, don't typically shift the current waveform, instead they distort it. These distorted waveforms can be broken into harmonic components using Fourier series. The harmonic currents produce no useful work and therefore reactive in nature. Non-linear loads are extremely prevalent on today's power systems and are typically the result of the rectifiers used to convert AC power to DC power in power electronics systems. Examples include variable speed drives, computers, broadcasting equipments, compact fluorescent and LED lighting, electrical chargers, induction furnaces etc. For non-linear loads the power vector relationship becomes three dimensional with distortion reactive power H combining with both Q and P to produce the apparent power which power system must deliver; unlike classical power triangle. Power factor remains the ratio of Watts to VA but now the VA has harmonic component as well. Here the true power factor becomes combination of displacement power factor and distortion power factor. Displacement power factor is still equals $\cos\theta$ with θ being the angle between fundamental current and voltage. Displacement power factor can be either leading or lagging. Distortion power factor is neither leading nor lagging. For typical non-linear loads the displacement power factor will be near unity. True power factor however, is normally very low due to distortion. For example the displacement power factor of variable speed drive will be near unity but its total power factor is often 0.7-0.8; unless harmonic mitigation circuits are employed.

Today, with heavy proliferation of non-linear loads, low power factor on power systems is often result of high distortion reactive power components and not by inductive (or capacitive) reactive power. Therefore one can no longer say that low power factor is normally caused by electric motors and other inductive loads. Since the best way to improve a poor power factor caused by non linear loads is to remove the harmonic currents the traditional means of adding power factor correction capacitor is quite no

longer suitable. In fact simply adding capacitors may often make the problem worse as they can resonate with the power system inductance.

The power supply to run all electronics systems for Control and Instrumentation (C&I) of Nuclear Power Plants are one of the most important components to enhance overall plant performance, [3], [6]. This aspect was realized by us, and thus from very basic the design which aimed for a rugged fault tolerant hot-pluggable, load sharing power supply was conceived and then engineered by ECIL and utilized in very large numbers in Nuclear Reactor Protection and Control Systems, for NPCIL plants, [1], [2], [4]. These are modular power Switched Mode Power Supplies (SMPS) are termed as 'Fault Tolerant Power Distribution System' (FTPDS). These are configured as M+N system, what we term as SMPS M+N configuration. The number M will cater total load, and number N are redundant units and all M+N sharing the load equally. Say our load is 185W, to cater that we use two (M) units of 100W and one (N) unit of 100W as redundant. Thus failure of one unit will not interrupt the load current. This configuration is therefore enhancing plant reliability and availability. This FTPDS (SMPS M+N) is Trade-Marked product [5] [8], [9] as ECPS^{TM} XX; like ECPS SM60 indicating 60W modules, ECPS SM100 indicating 100W modules. The latest embodiments [2],[8], [9] for NPCIL-PHWR700MW plant, is ECPS SM100 with two variants the first one is with DC-DC (input 220V DC), and second one is with AC-DC with input as 230V AC and this one having added circuits with boost convertor for Power Factor Correction (PFC) and Total Harmonic Distortion (THD) controls. For both embodiments output is regulated DC voltages of 5V, 12V, 15V, 24V. In this note we will report the power quality certification as per IEC 61000-3-2 standard, conducted on the latest embodiments, of ECPS SM100, for AC-DC models; and describe the circuit scheme to meet this objective. Presently about 10,000 numbers of ECPS100 are being fabricated for NPCIL-PHWR700MW. The detailed test results are kept in CAD NPP, ECIL-Hyderabad.

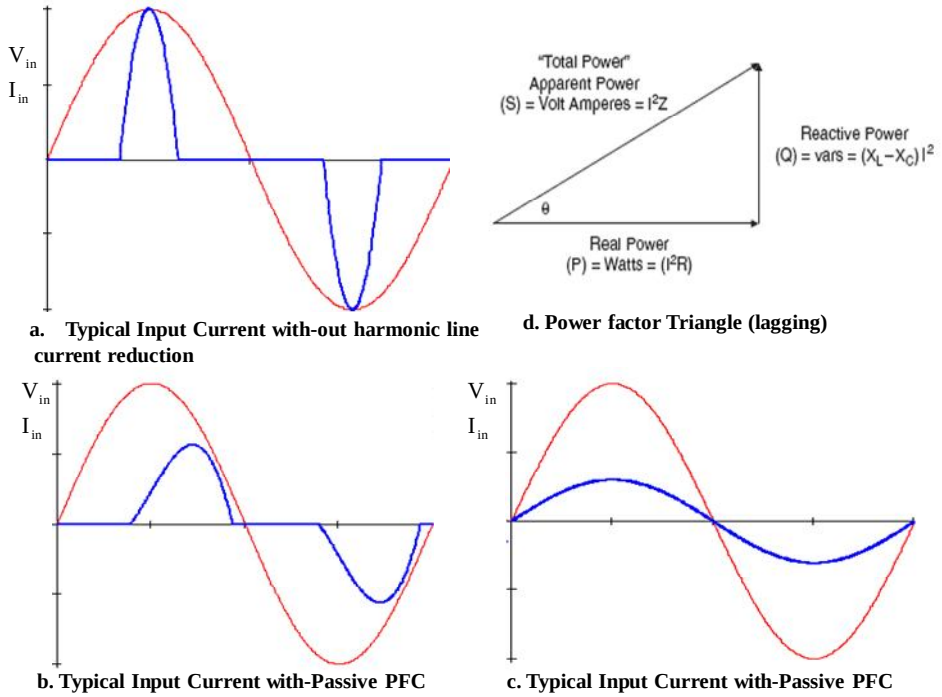
Power Quality Control Standard & Techniques

As of 2001, all electrical and electronic equipment that is connected to public mains up to and including 16A max, rated input current must comply with IEC 61000-3-2. Passive and active harmonic line current reduction solutions can be used to fulfill the limits of the standards which greatly influences the design of all power supplies. EN 61000-3-2 came into effect on 1995 and has replaced EN 60555-2 as on 2001. The last version of this standard has been accepted by CENELEC in 2006. It is based on IEC 61000-3-2:2005; in the meantime two amendments (A1:2008 and A2:2009) have been published. Since 2009 only IEC 61000-3-2: 2006 is applicable all older versions of EN-61000 are expired. The acceptable limits are displayed in the test results.

Harmonic line current reduction can be achieved by using different techniques. The most common techniques for harmonic current reduction are line filters, using passive components; and active electronics circuitry. Harmonic line current reduction technique using passive components (inductors and capacitors) introduces high impedance for harmonics thus smoothening the input current to electronic equipment.

Harmonic line current reduction using the active electronic circuitry is shaping the input current of electronic equipment proportional to the applied line voltage thus giving sinusoidal input current in phase with the line voltage. The corresponding electronic circuitry is called Power Factor Correction (PFC) circuitry; although power factor correction is not the correct wording but has become synonymous for harmonic line current reduction. The harmonic line current reduction using the passive components sometimes called passive PFC. The passive technique is also called Passive VAR Generators-that was earlier used in C&I systems, when the SMPS used did not have PFC Circuitry.

Figure-1 shows the principle of the AC line input current reduction. Without any harmonic current reduction circuitry the input current achieves very high limits as the current is only limited by the small input impedance (filter and cabling) of the power supply. Adding additional inductances (passive solution) reduce the input current as well as its harmonic contents. Best harmonic current reduction is achieved by active PFC. In our latest embodiment of ECPS SM 100 we have followed active PFC circuitry.



a. Typical Input Current with-out harmonic line current reduction

d. Power factor Triangle (lagging)

b. Typical Input Current with-Passive PFC

c. Typical Input Current with-Passive PFC

Figure-1: Line current with and without harmonic reduction circuitry

Passive harmonic line current reduction has advantage as; simple and robust circuitry; less costly than active PFC (Especially in 3-phase). Disadvantages are; large and heavy as low frequency magnetic needed; not applicable for wide input range & higher power; no sinusoidal input current. Active harmonic line current reduction has advantages as; extensive elimination of line current harmonics; Power Factor (PF) nearly unity (PF is about 0.6 for uncorrected system); and wide input voltage range possible. The disadvantages of active PFC are; requires additional expense circuitry; increased number of parts and has negative impact on power conversion efficiency (due to losses in switching technique used).

Harmonics & how are they related to power factor with some measurement parameters for Power Quality quantification defined

The real power (watts) produces real work; this is the energy transfer component (example electricity to run motor rpm). Reactive power is the power required to produce the magnetic fields (lost power), in lagging PF system; to enable the real work to be done; where apparent power is considered the total power that the C&I AC power distribution supplies. This total power is the power supplied through the power mains to produce the required amount of real power. The lagging power factor triangle is depicted in Figure 1d. This stated definition of power factor related to phase angle is valid when considering "ideal-sinusoidal" wave-forms for both current and voltage; however most power supplies draw a non-sinusoidal current. When the current is not sinusoidal and the voltage is sinusoidal, the power factor consists of two factors: 1) the displacement factor related to phase angle and 2) the distortion factor related to current wave shape. When the power factor is not equal to one, the current waveform does not follow the voltage waveform. This results not only in power losses but may cause harmonics that travel down the neutral line and disrupt other devises connected to the line. The closer the power factor is to one, the closer the current harmonics will be to zero since all the power is contained in the fundamental frequency. Therefore, the purpose of the power factor correction circuit is to minimize the input current distortion and make the current in phase with the voltage.

For Power Factor we take ratio of the Active Power in Watt (W) to Apparent Power in Volt-Ampere (VA); for the fundamental current.

$$\mathrm{pf}_{\mathrm{disp}} = \frac{\text{Active - Power (W)}}{\text{Apparant - Power (VA)}} \tag{1}$$

This is also called Displacement Power Factor ($\mathrm{pf}_{\mathrm{disp}}$). Whereas the True Power Factor ($\mathrm{pf}_{\mathrm{true}}$), is ratio of composite wave (current)-including all harmonics.

$$\mathrm{pf}_{\mathrm{true}} = \frac{\text{Total Active - Power (W)}}{\text{Total Apparant - Power (VA)}} \tag{2}$$

Thus we have $\mathrm{pf}_{\mathrm{true}} \le \mathrm{pf}_{\mathrm{disp}}$.

Total Harmonic Distortion (THD) is defined as (for current wave);

$$\mathrm{THD}_{\mathrm{I}} = \left(\sqrt{\sum_{n=2}^{40} \left(\frac{\mathrm{I}_n}{\mathrm{I}_1} \right)^2} \right) (100)\% \tag{3}$$

where I_n is, RMS value of higher harmonic components, and I_1 is the fundamental RMS value of the current. We will derive in next section and use this to define distortion power factor. IEC-61000-3-2 gives THD values taking 40 harmonic components. This parameter is important for non-linear loads and we will see how this causes poor 'true power factor', in spite of having classical displacement power factor as close to unity.

Crest Factor is defined as ratio of peak current to RMS current. This defines deviation from ideal sinusoid.

$$CF = \frac{I_{peak}}{I_{RMS}} \tag{4}$$

For ideal sinusoid this crest factor is $CF = \sqrt{2} = 1.414$; that is for pure sinusoid we have $I_{RMS} = \left(\frac{1}{\sqrt{2}}\right) I_{peak}$.

The test results of SMPS without PFC gives the PF is poor at 0.436 and poor crest factor of 4.65 (ideally it should be 1.414); and the current having large harmonic contents giving THD as 216.50%. This is for earlier embodiments of ECPS without PFC circuitry.

Derivation of true, distortion and displacement power factors for non-sinusoidal current

Voltage and currents harmonics produced by non-linear loads increase power losses and therefore have a negative impact on electric utility distribution systems and components. While the exact relationship between harmonics and losses is very complex and difficult to generalize, the well established concepts of power factor does provide some measure of the relationship, and useful when comparing the relative impacts of non-linear loads-providing that harmonics are incorporated into power factor definition [13].

The voltage and currents at the linear-load, with V_1 , I_1 representing the peak values of voltage and currents of 50 Hz and δ_1, φ_1 relative phase angles are

$$v(t) = V_1 \sin\left(\omega_0 t + \delta_1\right) \qquad i(t) = I_1 \sin\left(\omega_0 t + \varphi_1\right) \tag{5}$$

The subscript one indicates 'fist-harmonic' the fundamental component. The true power factor at the load is determined as the ratio of the average power to the apparent power

$$pf_{true} = \frac{P_{avg}}{S} = \frac{P_{avg}}{V_{RMS} I_{RMS}} \tag{6}$$

For purely sinusoidal case the above becomes (Figure-1d)

$$pf_{true} = pf_{disp} = \frac{P_{avg}}{\sqrt{P^2 + Q^2}} = \frac{\frac{V_1}{\sqrt{2}} \frac{I_1}{\sqrt{2}} \cos\left(\delta_1 - \varphi_1\right)}{\frac{V_1}{\sqrt{2}} \frac{I_1}{\sqrt{2}}}$$

$$= \cos\left(\delta_1 - \varphi_1\right) = \cos\theta_1 \tag{7}$$

$$\theta_1 = \delta_1 - \varphi_1$$

The subscript one implies "fundamental" component. Here, pf_{disp} is commonly known as the displacement power factor; with $\theta_1 = \delta_1 - \varphi_1$ is known as power factor angle. Thus for sinusoidal cases there is only one power factor because true power factor and displacement power factor are equal. For sinusoidal situations unity power factor corresponds to zero reactive power Q, and low power factor corresponds to high Q. Since most loads consume reactive power, low power factor in sinusoidal systems can be corrected by simply shunt capacitors.

Now consider non-sinusoidal cases, where network voltages and currents contain harmonics. While some harmonics are caused by system nonlinearities such as transformer saturation, most harmonics are produced by switched systems of power electronics, as adjustable speed drives, diode-bridge rectifiers. The significant harmonics (above the fundamental i.e. the first harmonic) are usually 3rd, 5th, and 7th multiples of 50Hz, so the frequencies of interest in harmonics studies are in low-audible range. When steady-state harmonics are present, voltages and currents may be represented by Fourier series in following form.

$$v(t) = \sum_{k=1}^{\infty} V_k \sin\left(k\omega_0 t + \delta_k\right) \qquad i(t) = \sum_{k=1}^{\infty} I_k \sin\left(k\omega_0 t + \varphi_k\right) \tag{8}$$

Whose RMS values can be written as following expressions

$$V_{RMS} = \sqrt{\sum_{k=1}^{\infty} V_{kRMS}^2} = \sqrt{\sum_{k=1}^{\infty} \frac{V_k^2}{2}} \qquad I_{RMS} = \sqrt{\sum_{k=1}^{\infty} I_{kRMS}^2} = \sqrt{\sum_{k=1}^{\infty} \frac{I_k^2}{2}} \tag{9}$$

The average power is given by

$$\begin{aligned} P_{avg} &= \sum_{k=1}^{\infty} V_{kRMS} I_{kRMS} \cos\left(\delta_k - \varphi_k\right) = \sum_{k=1}^{\infty} V_{kRMS} I_{kRMS} \cos\theta_k \\ &= P_{1avg} + P_{2avg} + P_{3avg} + ... \end{aligned} \tag{10}$$

where we see that each harmonic makes a contribution plus or minus to the average power. Commonly used parameter of harmonic levels is Total Harmonic Distortion THD (or Distortion Factor), which is the ratio of the RMS value of the harmonic (above fundamental) to the RMS value of the fundamental times 100% i.e.

$$\begin{aligned} THD_I &= \frac{\sqrt{\sum_{k=2}^{\infty} I_{kRMS}^2}}{I_{1RMS}}(100)\% = \frac{\sqrt{\sum_{k=2}^{\infty} I_k^2}}{I_1^2}(100)\% \\ THD_V &= \frac{\sqrt{\sum_{k=2}^{\infty} V_{kRMS}^2}}{V_{1RMS}}(100)\% = \frac{\sqrt{\sum_{k=2}^{\infty} V_k^2}}{V_1^2}(100)\% \end{aligned} \tag{11}$$

The above expressions of THD are for non-sinusoidal current and voltage wave-forms. Obviously when the case is of pure sinusoid there are no harmonics and THD is zero. Using the earlier expression (9) i.e. $I_{RMS} = \sqrt{\sum_{k=1}^{\infty} I_{kRMS}^2} = \sqrt{I_{1RMS}^2 + I_{2RMS}^2 + ...}$ and by use of above definition (11) of THD we write the following

$$I_{RMS} = I_{1RMS}\sqrt{1 + \left(THD_I / 100\right)^2} \qquad V_{RMS} = V_{1RMS}\sqrt{1 + \left(THD_V / 100\right)^2} \tag{12}$$

Now substituting the above expressions into (6) i.e. $pf_{true} = P_{avg} / S = P_{avg} / V_{RMS} I_{RMS}$ get expression for true power factor for non-sinusoidal case as

$$\begin{aligned} pf_{true} &= \frac{P_{avg}}{V_{1RMS} I_{1RMS} \sqrt{1 + \left(THD_V / 100\right)^2}\sqrt{1 + \left(THD_I / 100\right)^2}} \\ &= \left(\frac{P_{avg}}{V_{1RMS} I_{1RMS}}\right)\left(\frac{1}{\sqrt{1 + \left(THD_V / 100\right)^2}\sqrt{1 + \left(THD_I / 100\right)^2}}\right) \end{aligned} \tag{13}$$

We make two assumptions: (a) in most cases, the contributions of harmonics above the fundamental to average power in the expression (10) that is $P_{avg} = \sum_{k=1}^{\infty} V_{kRMS} I_{kRMS} \cos(\delta_k - \varphi_k) = P_{1avg} + P_{2avg} + P_{3avg} + ...$ are small so we take $P_{avg} \approx P_{1avg}$. (b) Since THD_V is usually less than 10% then from the expression (12) that is $V_{RMS} = V_{1RMS}\sqrt{1+(THD_V/100)^2}$ we write $V_{RMS} \approx V_{1RMS}$. This gives following simplified expression

$$pf_{true} \approx \left(\frac{P_{1avg}}{V_{1RMS} I_{1RMS}}\right)\left(\frac{1}{\sqrt{1+(THD_I/100)^2}}\right) = (pf_{disp})(pf_{dist}) \qquad (14)$$

Because displacement power factor pf_{disp} can never be greater than one, the above expression shows that true power factor in non-sinusoidal case has upper bound as

$$pf_{true} \le pf_{disp} = \frac{1}{\sqrt{1+(THD_I/100)^2}} \qquad (15)$$

The above equation (15) is plotted in Figure-2 provides insight into nature of true power factors of power electronic loads, especially single-phase loads. Single-phase power electronics loads such as desktop computers and home entertainment equipments tend to have high current distortions near 100%. Therefore their true power factor is generally less than 0.7071; that is $1/\sqrt{2}$ even their displacement power factor is close to unity. On the other hand, three-phase power electronic loads inherently have lower current distortions than single-phase loads, thus higher distortion power factor. However if three phase loads employ phase control their true power factors may be poor at reduced load levels due to low displacement power factors.

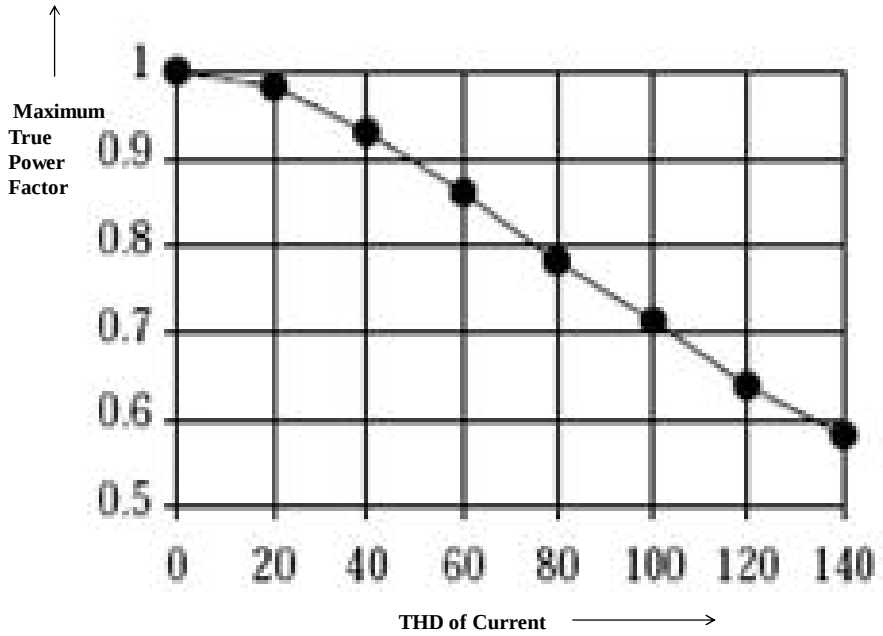


Figure-2: Maximum true power factor vs. THD of current

It is important to point out that one cannot in general compensate for poor distortion power factor by adding shunt capacitors. Only the displacement power factor can be improved with capacitors. This fact is especially important in load areas that are dominated by single phase power electronic loads, which tend to have high displacement power factor but low distortion power factors. In these instances the addition of shunt capacitors will likely worsen the power factor by inducing resonances and higher harmonic levels. A better solution is to add passive or active filters to remove the harmonics produced by non-linear loads, or utilize low distortion power electronic loads.

Type of Load	pf_{disp}	THD_I	pf_{dist}	pf_{true}
Ceiling Fan	0.999	1.8	1.000	0.999
Refrigerator	0.875	13.4	0.991	0.867
Vacuum Clean	0.951	26.0	0.968	0.921
μ-Wave Oven	0.998	18.2	0.984	0.982
CFL Lighting	0.956+	39.5	0.930	0.889
Television	0.988+	121.0	0.637	0.629
Computers	0.999+	140.0	0.581	0.580

Table-1: Power Factor & Current Distortion Measurement for common single-phase house-hold loads

Table-1 gives the displacement power factor, THD of current, distortion power factor and true power factor for various home appliances. The plus sign above in the Table-1 entries for few loads indicate leading displacement power factor corresponding to these loads.

For non-linear loads the power vector relationship becomes three dimensional with distortion reactive power H combining with both Q and P to produce the apparent power which power system must deliver; depicted in Figure-3 (unlike classical Figure-1d). Power factor remains the ratio of Watts to VA but now the VA has harmonic component as well. As described above, the true power factor becomes combination of displacement power factor and distortion power factor. Displacement power factor is still equals $\cos\theta$ with θ being the angle between fundamental current and voltage. Displacement power factor can be either leading or lagging. Distortion power factor is neither leading nor lagging. For typical non-linear loads the displacement power factor will be near unity. True power factor however, is normally very low due to distortion. For example the displacement power factor of variable speed drive will be near unity but its total power factor is often 0.7-0.8; unless harmonic mitigation circuits are employed.

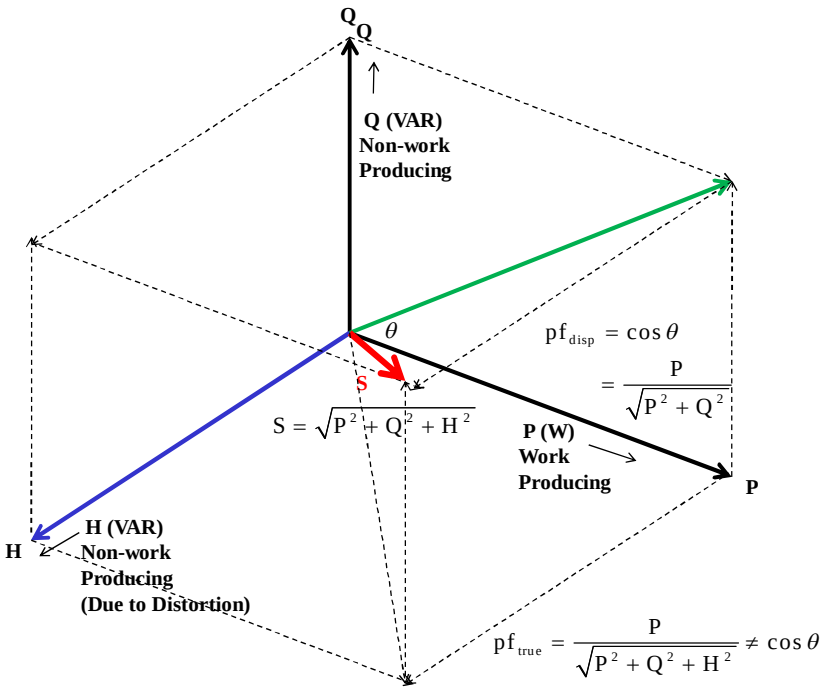


Figure-3: Three Dimensional Representation of True Power Factor

Need for Power Factor Control and Harmonic Reduction for SMPS

To understand the nature of power factor and its various effects and to provide a foundation for understanding how it impacts the AC power distribution system, some back ground on the complex issue of power factor is necessary. In an AC system, the generation source establishes a sinusoidal voltage waveform, and the load establishes the current waveform. In the simplest case of so-called "resistive" load like heater or incandescent bulb, the current wave form is the same shape as the voltage waveform and lines up precisely with time. The product of the voltage and the current at every instant of time is always positive. By definition the resistive load is said to have a power factor of one, meaning that 100% of the load current contributes to the watts of power transferred to the load. In an ideal world all loads would have power factor of one.

However, many types of electrical loads draw some currents that do not contribute to the watts of power transferred to the load. These are generally undesirable currents that do not transfer watts because they are not aligned in time with the voltage waveform (they are out-of-phase currents), or they are of a different frequency than the source voltage (they are harmonic currents). Let us have two waveforms (voltage & current) of the same shape of sinusoid (i.e. no harmonic currents) where the current wave form is 90 degree ahead of voltage waveform. In this case instantaneous product of voltage and current is positive half the time and negative half the time, meaning that the power delivered to the load is alternating between positive and negative, with an average watt value zero. When the current is out of phase with voltage (90 degrees leading or lagging), no average power is delivered to the load.

An actual load current can be separated into three parts: a part that is in phase with the voltage (the part that transfer watts); a part that is out-of phase (a part that does not transfer watts); and a part that carries harmonics (also does not transfer watts). The ratio of the part of the load current that transfers watts to the load divided by the total current (including out of phase and harmonic currents) is called the power factor. Therefore, the power factor of a load is always between zero and one, with one power factor meaning that all the current is going towards delivery of power to the load; and zero power factor meaning that no part of current is going towards delivery of power to the load (i.e. it is all out-of-phase or harmonic currents).

Both out-of-phase and harmonic currents contribute to reduction in power factor from the ideal value of one and can cause problems in C&I systems. Both cause wire, transformers and circuit breakers to need to be oversized to handle the additional currents. However, harmonic currents create additional unique problems such as excessive heating in transformers, motors, and can cause overheating of the neutral wire. The out-of-phase part of the current, which technically defined as the “reactive current”, can affect voltage regulation in the AC power systems of C&I systems. A great deal of confusion regarding the subject of power factor is the failure to recognize that the two different types of currents that contribute to reduction in power factor namely the harmonic and the reactive currents, can cause different problems. Unfortunately when a load is described as having a “power factor of 0.8” it really tells us nothing about whether the currents causing the value to be different than one are harmonic currents or reactive currents.

Without using Power Factor Correction (PFC) circuitry a typical SMPS has True PF around 0.45, therefore having considerable harmonics distortion. Having a power factor less than one along with harmonics from peaky loads reduces the real power available to run the device. In order to operate a device with these inefficiencies, the power distribution network of plant C&I must supply additional power to make up for losses. This increase in power causes the AC power networks to use heavier supply lines, otherwise self-heating can cause burnout in the neutral line conductor. The harmonic distortion can cause an increase in operating temperature of the generation facility, which reduces the life of the equipment including rotating machines, cables, transformers, capacitors, fuses, switching contacts, and surge suppressors. Problems are caused by the harmonics creating additional losses and dielectric stress in capacitors and cables,

increasing currents in windings of rotating machinery and transformers and noise emission in many products, and bringing about early failure of fuses and other safety components. They can also cause skin effect, which creates problems in cables, transformers and rotating machines.

The Boost Converter is the Main element of Active Power Factor Correction

Boost converter is used to accomplish the active PFC in many discontinuous/continuous conduction modes (DCM/CCM). First we see how the inductors can produce very high voltages-is depicted in Figure-4. Initially the inductor is assumed to be uncharged, so the voltage V_0 is equal to V_{in}. When the switch closes, the current I_L gradually increases linearly as $I_L = \frac{1}{L}\int V_L dt$. Voltage V_L across it increases exponentially (that is by considering small resistance of inductor) until it stabilizes at V_{in}. Notice the polarity of the voltage across the inductor, as it is defined by the current direction (in side taken as positive). When the switch opens that cause the current to change from I_{max} to zero (which is a decrease, or a negative slope). That is L times the change in current per unit time, the voltage approaches negative infinity (the inductor reverses the polarity).

$$V_L = L\frac{di}{dt} \approx L\frac{\Delta i}{\Delta t} \tag{16}$$

Since the inductor is not ideal, it contains some amount of series resistance, which loads this "infinite" voltage to a finite value. With the switch open and inductor discharging, the voltage across it reverses and becomes additive with the source voltage V_{in}. If a diode and capacitor were connected to the output of this circuit, the capacitor would charge to this high voltage (after few switching cycles). This is the operation of Boost Converter (Figure-5). The high stored voltage on the capacitor charged during the fly-back operation, delivers the reactive power to subsequent power converter circuit-i.e. Buck Converter of SMPS. Thus the reactive power required for magnetization of the inductors of the subsequent stage is delivered by this boost converter's boosted DC voltage (in our circuit it is at 390V DC).

The input to the converter is full rectified AC line voltage. No bulk filtering is applied following is applied following the bridge rectifier, so the input voltage to the boost converter ranges (at twice the line frequency) from zero volts to peak value of the AC input and back to zero. The boost converter must meet two conditions simultaneously; 1) the output voltage of the boost converter must be set higher than the peak value (hence the word boost) of the line voltage (we used 390V DC to allow high line voltage 265V RMS); 2) the current drawn from the line at any given instant must be proportional to the line voltage. In Figure-5 the Boosted DC Voltage (390V DC) of this PFC stage goes to the second stage of power converter circuit, which is a current mode PWM DC-DC (Buck Converter) converter of ECPS circuit, operating on 80 KHz. The Figure-5 circuit is pre-Boosted converter which operates on Fixed Frequency 100 KHz. This complete set is for latest embodiment of ECPS 100W system.

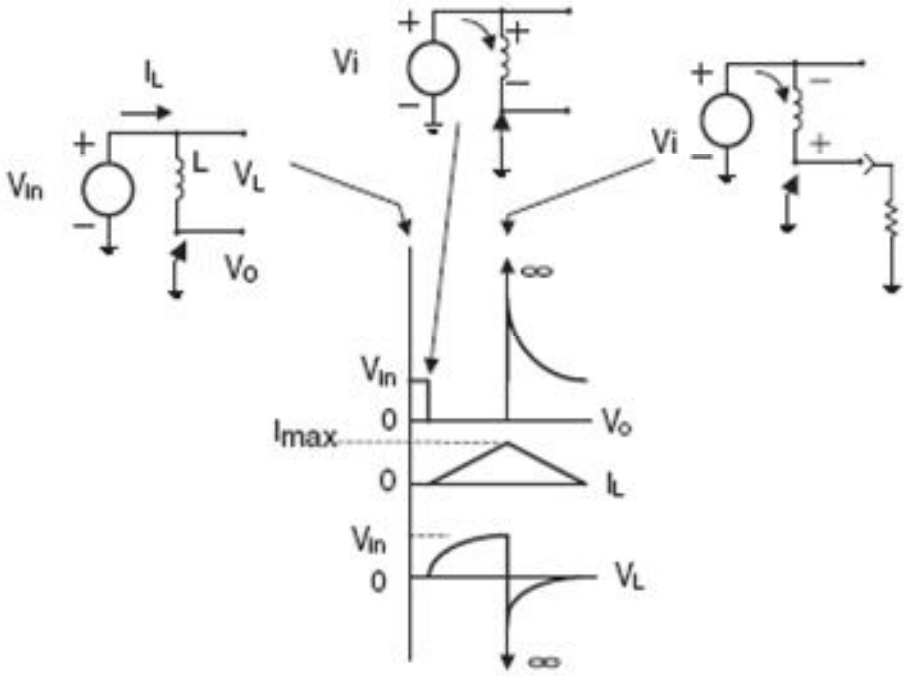


Figure-4: Fly back operation of Inductor

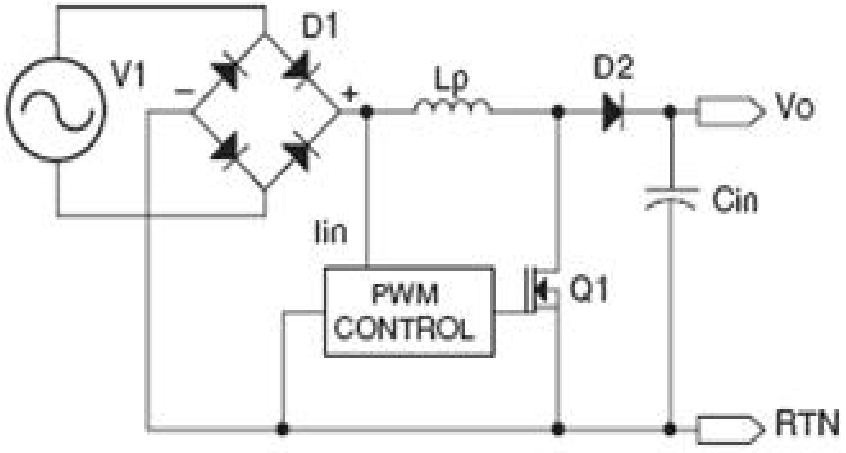
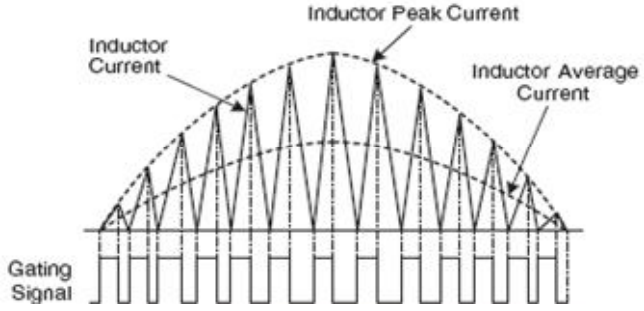


Figure-5: Boost Converter Circuit

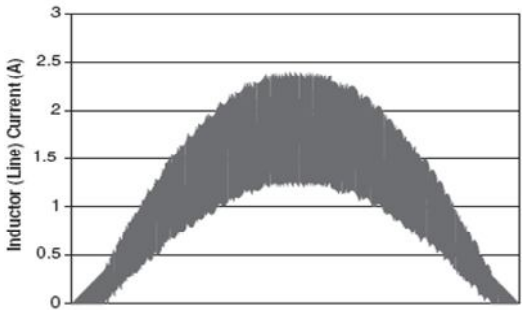
This is why power companies are concerned with growth of SMPS that will cause THD levels to increase to unacceptable levels. Having the boost pre-converter voltage higher than the input voltage forces the load to draw current in phase with AC line-voltage that in turn reduces the harmonic emissions.

Active Power Factor Correction (PFC) Schemes as per IEC61000-3-2

There are two modes of PFC operation; discontinuous and continuous mode (DCM and CCM). Discontinuous mode is when the boost converter MOSFET is turned on when the inductor current reaches zero, and tuned off when the inductor current meets the desired input reference voltage as shown in Figure-6a. In this way the current waveform follows that of the input voltage, thus attaining PF close to one. Discontinuous Mode is used for SMPS that have power levels of 300 W or less, like LED Control. In comparison with continuous mode devices the discontinuous mode uses larger cores and have higher I^2R and skin effect losses due to larger swings of inductor current. With the increased swing a larger input filter is also required. On the positive side since discontinuous mode devices switch the boost MOSFET on when the inductor current is zero, reducing the switching loss and there is no reverse recovery current I_{RR} specification required on the boost diode.



a. Discontinuous Mode



b. Continuous Mode

Figure-6: Modes of operation of Active PFC

In the figure-6a the AC line current is shown continuous waveform where the peak switch current is twice the average input current. In this mode, the operation frequency varies with constant on time.

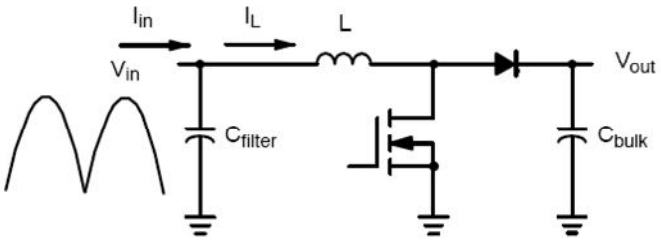
Continuous mode which is also called Average Current Mode typically suits SMPS power levels greater than 300W. This is where the boost converter's MOSFET does not switch on when boost inductor is at zero current, instead the current in the energy transfer inductor never reaches zero during the switching cycle. This is depicted in Figure-6b. With this in mind the voltage swing is less than in discontinuous mode-resulting in lower I^2R losses and lower ripple current results in lower inductor core losses. Less voltage swing also reduces EMI and allows for smaller input filter to be used. Since MOSFET is not turned on when the boost inductor current is zero, a very fast reverse

recovery diode is required to keep losses to minimum. In our PFC we used continuous mode.

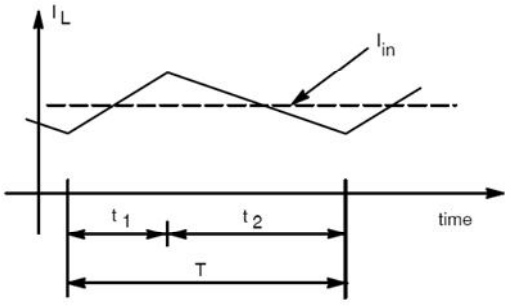
Fixed Frequency Continuous Mode for PFC in SMPS (M+N)

In the latest embodiment of ECPS, Power Factor Correction (PFC) boost controller is operated in circuit in fixed-frequency Continuous Conduction Mode (CCM) or Average Current Mode. Fixed frequency operation eases the compliance with EMI standards and the limitation of possible radiated noise that may pollute surrounding systems. The CCM operation reduces the application of di/dt and the resulting interference. A CCM PFC boost converter is shown in Figure-7a. The input voltage is rectified 50 Hz sinusoidal signal. The MOSFET is switching at a high frequency (100 KHz) so that inductor current I_L basically consists of high and low frequency components. Filter capacitor C_{filter} is essential and very small value capacitor in order to eliminate the high-frequency component of the inductor current I_L. This filter capacitor cannot be too bulky because it can pollute the power factor by distorting the rectified sinusoidal input voltage. As shown in Figure-7b, the inductor current I_L in a switching period T includes a charging phase for duration t_1 and discharging phase for duration t_2. The voltage conversion ratio is obtained by following relation

$$\frac{V_{out}}{V_{in}} = \frac{t_1 + t_2}{t_2} = \frac{T}{T - t_1}; \qquad V_{in} = \frac{T - t_1}{T} V_{out} \tag{17}$$



a. Boost Converter of CCM PFC



b. Inductor Current in CCM

Figure-7: Boost Converter and Inductor Current

The input filter capacitor C_{filter} and the front-ended EMI filter absorb the high-frequency component of inductor current I_L. It makes the input current I_{in} a low-frequency signal only of the inductor current

$$I_{in} = I_{L-50} \tag{18}$$

The suffix 50 means it is with a 50 Hz bandwidth of the original I_L. From above expressions we write

$$Z_{in} = \frac{V_{in}}{I_{in}} = \frac{T - t_1}{T} \frac{V_{out}}{I_{L-50}} \tag{19}$$

Power Factor is corrected when the input impedance Z_{in} is constant or slowly varying in the 50 Hz bandwidth-i.e. Z_{in} behaves as resistive quantity.

a. CCM PFC Duty Modulation

b. CCM PFC Timing Diagram

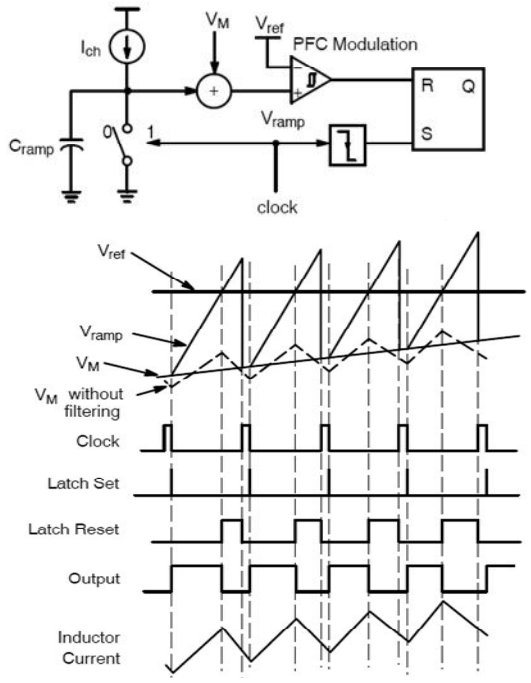


Figure-8: CCM PFC Duty Modulation and Timing Diagram

The PFC duty modulation and timing diagram is shown in Figure-8. The MOSFET on time t_1 is generated by the intersection of reference voltage V_{ref} and ramp voltage V_{ramp}. A relationship is following (comes from circuit of Figure-8a)

$$V_{ramp} = V_M + \frac{I_{ch}}{C_{ramp}} t_1 = V_{ref} \tag{20}$$

The charging current I_{ch} is specially designed as

$$\begin{aligned} I_{ch} &= \frac{C_{ramp} V_{ref}}{T} \\ V_M &= V_{ref} - \frac{t_1}{C_{ramp}} \frac{C_{ramp} V_{ref}}{T} = V_{ref} \frac{T - t_1}{T} \end{aligned} \tag{21}$$

From above set of equations (19)-(21) we get input impedance as re-formulated as

$$Z_{in} = \frac{V_M}{V_{ref}} \frac{V_{out}}{I_{L-50}} \tag{22}$$

Because V_{ref} and V_{out} are roughly constant with time, the multiplier voltage V_M is designed to be proportional to I_{L-50} in order to have constant Z_{in} for PFC purpose, is shown in Figure-9.

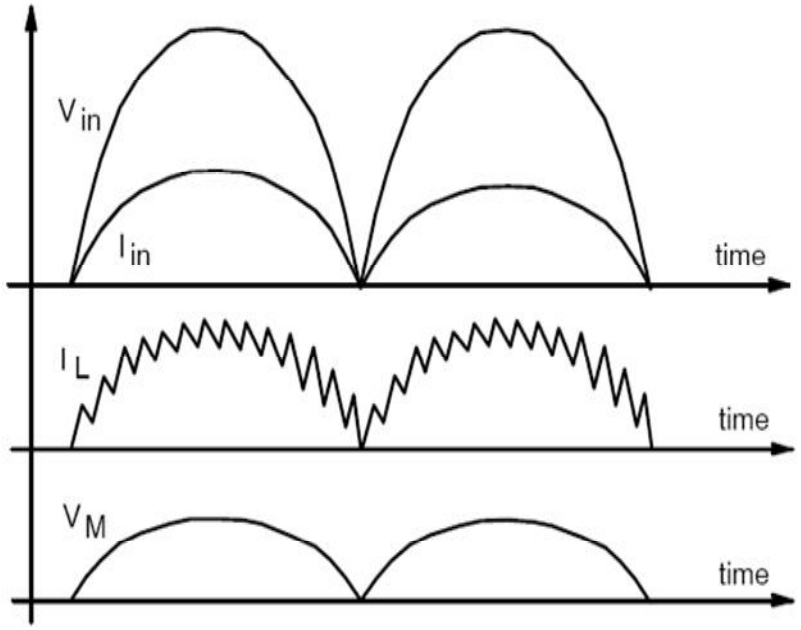


Figure-9: Multiplier Voltage Timing Diagram

The multiplier voltage V_M is generated by sensing the input current via inductor current consisting of switching frequency ripple (that comes from inductor current I_L). The duty ratio can be inaccurately generated due to this ripple. This modulation is so called-"peak current mode". With the help of a filter capacitor C_M for filtering multiplier voltage V_M to bypass high-frequency ripple-the modulation becomes-"average current mode" (Figure-10). The multiplier voltage V_M gets generated by formula

$$V_M = \frac{R_M I_{Vac} I_S}{2 I_{control}} \tag{23}$$

Input-voltage current i.e. I_{Vac} is proportional to the RMS input voltage V_{ac} described by following expression (will be described later with circuit)

$$I_{Vac} = \frac{\sqrt{2}V_{ac} - 4V}{R_{Vac} + 12k\Omega} \approx \frac{V_{ac}}{R'_{Vac}} \tag{24}$$

The suffix stands for the RMS. I_{Vac} is a constant in 50Hz band-width. Multiplier resistor R_M is the external resistor connected as shown in Figure-10; it is also a constant. This

resistor R_M directly limits the maximum input power capability and its value affects the capability of the PFC controller to operate on either “follower boost mode” or “constant output voltage mode”

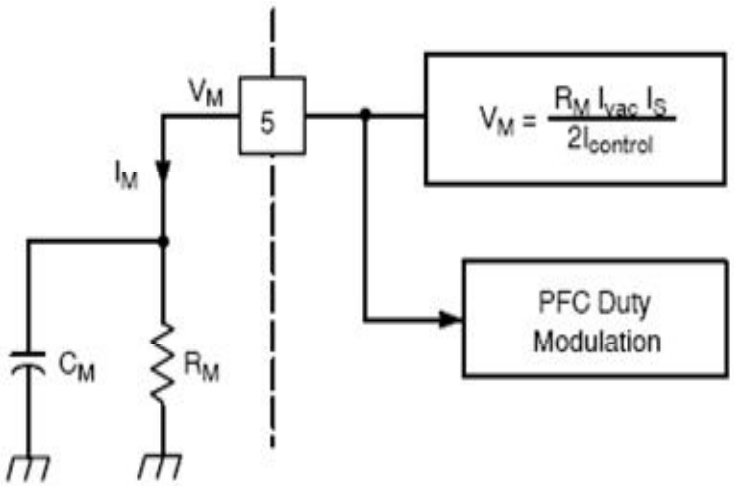


Figure-10: Placing filter capacitor for multiplier voltage

Sense current I_S is proportional to the inductor current I_L as described by following expression(will be described later with circuit)

$$I_S = \frac{R_{CS}}{R_S} I_L \tag{25}$$

This I_L consists of the high frequency component (which depends on di/dt or inductor L) and low-frequency component which is $I_{L\text{-}50}$. Control current $I_{control}$ is roughly constant current that comes from PFC output voltage V_{out} that is slowly varying signal. The band-width of $I_{control}$ can be additionally limited by inserting an external capacitor $C_{control}$ to the control voltage $V_{control}$ point (Figure-11). To limit $f_{control}$ below 20Hz typically to achieve power factor correction purpose a $0.1\mu F - 0.33\mu F$, of $C_{control}$ will do.

$$C_{control} > \frac{1}{2\pi 300k\Omega f_{control}} \tag{26}$$

From the above equations (22)-(25) we get new formulation for Z_{in} as

$$\begin{aligned} Z_{in} &= \frac{R_M C_{CS} V_{ac} V_{out} I_L}{2R_S R'_{Vac} I_{control} V_{ref} I_{L-50}} \\ &= \frac{R_M C_{CS} V_{ac} V_{out}}{2R_S R'_{Vac} I_{control} V_{ref}} \qquad \text{when} \qquad I_L = I_{L-50} \end{aligned} \tag{27}$$

The multiplier capacitor C_M is the one to filter the high frequency components of the multiplier voltage V_M. The high-frequency component is basically coming from the inductor current I_L. On the other hand the filter capacitor C_{filter} of Figure-7a similarly removes the high frequency component of the inductor current I_L. If the capacitors C_M and the capacitor C_{filter} match with each other in terms of filtering capability, I_L becomes $I_{L\text{-}50}$. Input impedance Z_{in} is roughly constant in the bandwidth of 50Hz.

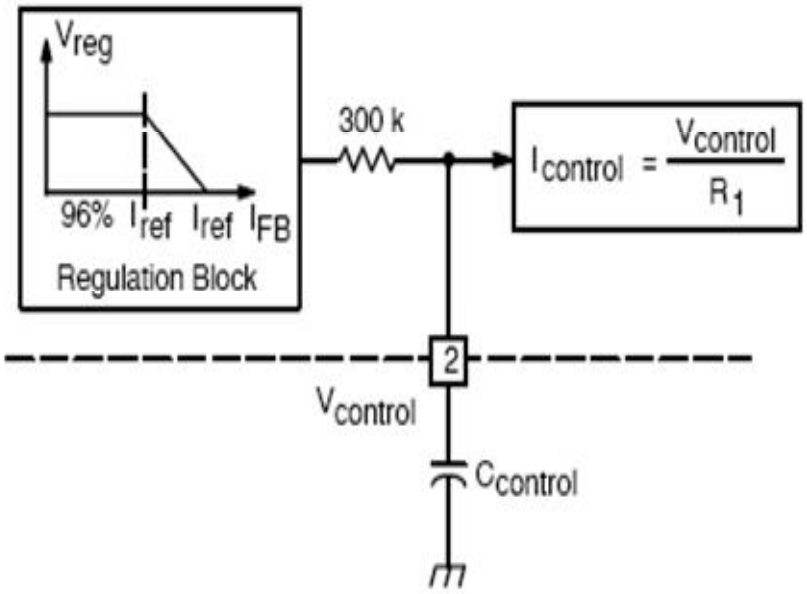


Figure-11: Low-pass filtering of $V_{control}$

Practically the differential-mode inductance in the front end EMI filter improves the filtering performance of the capacitor C_{filter}. Therefore the multiplier capacitor C_M is generally with a larger value comparing to the filter capacitor C_{filter}.

Input and output power is expressed in following expression; when the circuit efficiency η is obtained or assumed. The variable V_{ac} is RMS input voltage.

$$\begin{aligned} P_{in} &= \frac{V_{ac}^2}{Z_{in}} = \frac{2R_S R'_{Vac} I_{control} V_{ref} V_{ac}}{R_M R_{CS} V_{out}} \\ &\propto \frac{I_{control} V_{ac}}{V_{out}} \\ P_{out} &= \eta P_{in} = \eta \frac{2R_S R'_{Vac} I_{control} V_{ref} V_{ac}}{R_M R_{CS} V_{out}} \\ &\propto \frac{I_{control} V_{ac}}{V_{out}} \end{aligned} \tag{28}$$

The Follower Boost Mode

The PFC Controller operates on follower boost mode when $I_{control}$ is constant. If $I_{control}$ is constant then the expression of input and out put power as stated just above; for a constant load or power demand the output voltage V_{out} of the converter is proportional to the RMS input voltage V_{ac}. It means that the output voltage V_{out} becomes lower when RMS input voltage V_{ac} becomes lower. On the other hand the output voltage V_{out} becomes lower when the load or power demand becomes higher as in Figure-12.

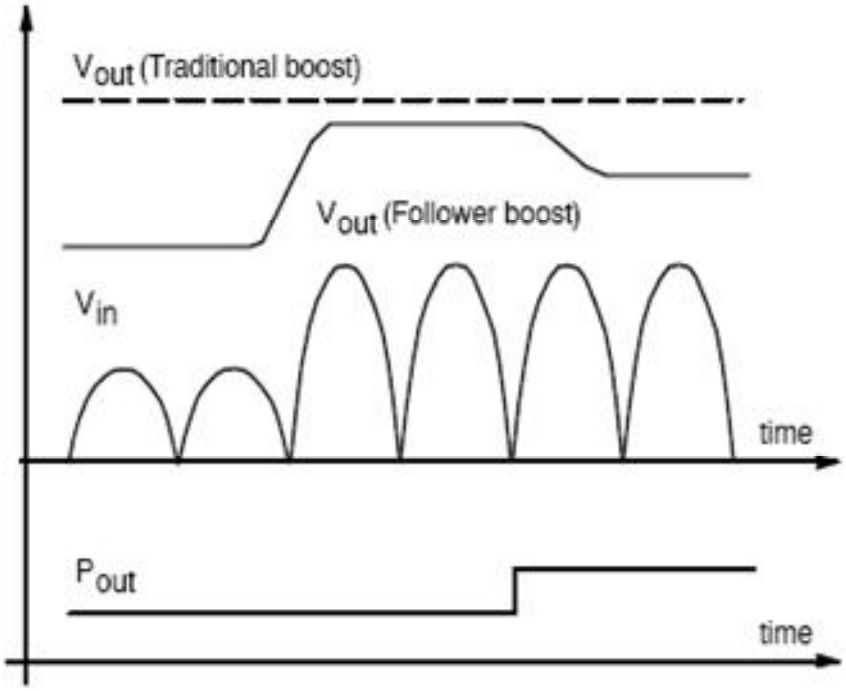


Figure-12: The Follower Boost Mode Characteristics

The follower boost circuit offers an opportunity to reduce the output voltage V_{out} whenever the RMS input voltage V_{ac} is lower or the power demand P_{out} is higher. Because of the step up property of the Boost Converter, the output voltage V_{out} will always be higher than the V_{in} even though V_{out} gets reduced in follower boost mode.

Output Feedback and Regulation

The output voltage V_{out} of the PFC circuit is sensed as a feedback current I_{FB} following into the feed-back point of PFC controller (Figure-13). Since the FB pin voltage V_{FB1} is much smaller than the V_{out}, it is usually neglected.

$$I_{FB} = \frac{V_{out} - V_{FB1}}{R_{FB}} \approx \frac{V_{out}}{R_{FB}} \tag{29}$$

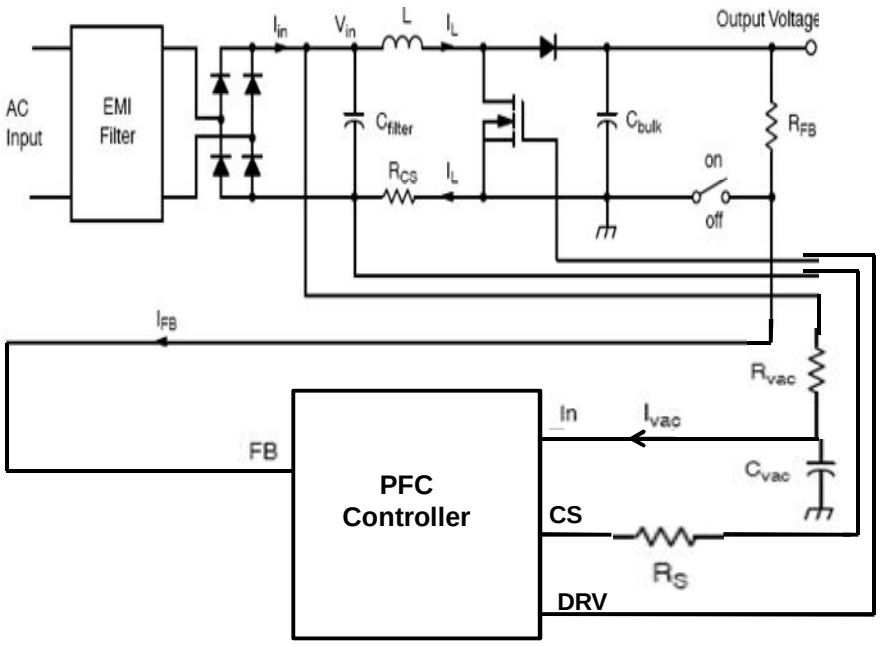


Figure-13: Output Feed-Back to PFC Controller

The resistor R_{FB} is the feedback resistor at FB point of the PFC Controller. Then the feedback current I_{FB} represents the output voltage V_{out} and is used for output voltage regulation and also under-voltage protection (UVP) and over-voltage protection (OVP).

Feedback current I_{FB} which represents the output voltage V_{out} is processed in a function with a reference current $I_{ref} = 200\mu A$, as shown in Figure-14. The output of the voltage regulation bock, low-pass filter on $V_{control}$ point of the PFC Controller, and the $I_{control} = V_{control} / R_1$ block of Figure-11 is control current $I_{control}$; and input feed-back current I_{FB}. It means that $I_{control}$ is the output of the I_{FB} and it can be described as in Figure-14. There are three linear regions including (a)- $I_{FB} < 96\%(I_{ref})$, (b)- $96\%(I_{ref}) < I_{FB} < I_{ref}$ and (c)- $I_{FB} > I_{ref}$.

When I_{FB} is less than $96\%(I_{ref})$ i.e. $V_{out} < 96\%(R_{FB} I_{ref})$, the PFC Controller operates in Follower Boost Mode. The Regulation Block output V_{reg} is at maximum value. $I_{control}$ becomes its maximum value (i.e. $I_{control} = I_{control(max)} = I_{ref} / 2 = 100\mu A$). We have following equation modified from power output equation (28) described previously.

$$V_{out} = \eta \frac{2 R_S R'_{Vac} I_{control(max)} V_{ref} V_{ac}}{R_M R_{CS} P_{out}} \propto \frac{V_{ac}}{P_{out}} \qquad (30)$$

The output voltage gets V_{out} is regulated at a particular level with particular value of RMS input voltage V_{ac} and output power. However, the output level is not constant and depends on different levels of V_{ac} and P_{out}, depicted in Figure-15a

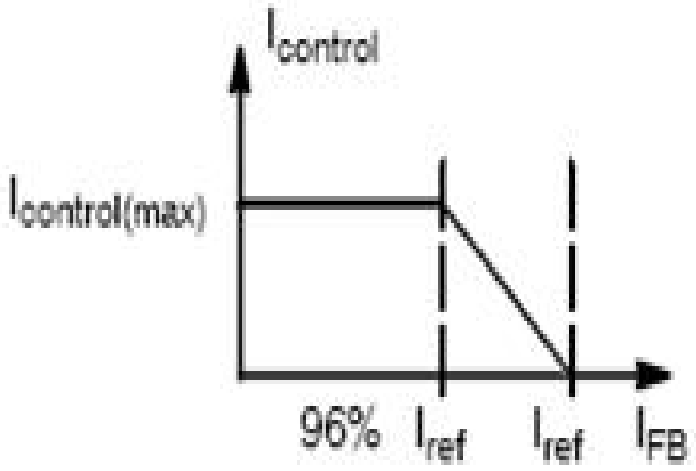


Figure-14: Regulation Block (Function)

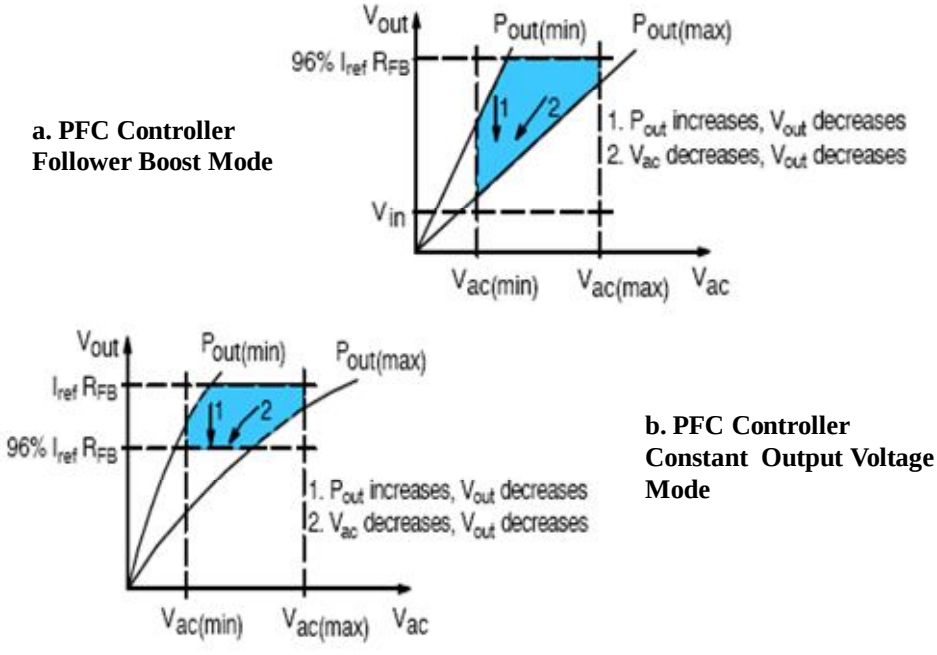


Figure-15: Modes of Operation of PFC Controller Regulation Block

When I_{FB} is between 96% and 100% of I_{ref} i.e. $96\%\left(R_{FB}I_{ref}\right) < V_{out} < R_{FB}I_{ref}$ the PFC controller operates in constant output voltage mode which is similar to the follower boost mode characteristics but with narrow output voltage range. The regulation block output V_{reg} decreases linearly with I_{FB} in the range of $0.96I_{ref}$ to I_{ref}. It gives linear function of $I_{control}$ described below.

$$I_{control} = \frac{I_{control(max)}}{0.04}\left(1 - \frac{V_{out}}{R_{FB}I_{ref}}\right) \tag{31}$$

Resolving to output power equation (28) as expressed earlier we get following

$$V_{out} = \frac{V_{ac}}{\left(\frac{R_M R_{CS}}{2R_S R'_{Vac} V_{ref}} \frac{0.04}{I_{control(max)}} \frac{P_{out}}{\eta} + \frac{V_{ac}}{R_{FB}I_{ref}}\right)} \tag{32}$$

According to the above equation (32), output voltage V_{out} becomes $R_{FB}I_{ref}$ when power is low ($P_{out} \approx 0$). It is the maximum value of V_{out} in this operating region. Hence, it can be concluded that output voltage increase when power decreases. It is similar to the follower boost mode (refer corresponding characteristic equation (32) above for follower boost mode). On the other hand the equation (32) just described above says output voltage V_{out} becomes $R_{FB}I_{ref}$ when RMS input voltage V_{ac} is very high. It is the maximum value of V_{out} in this mode of operation of PFC Controller. Hence it can also be concluded that output voltage increases when RMS input voltage increases. It is similar to another follower boost characteristic and is illustrated in Figure-15b.

When I_{FB} is greater than I_{ref} i.e. $V_{out} > R_{FB}I_{ref}$, the PFC Controller provides no output or zero duty ratio. Here V_{reg} become zero Volts, and $I_{control}$ also becomes zero. The multiplier voltage V_M in equation (23) i.e. $V_M = \frac{R_M I_{Vac} I_S}{2I_{control}}$ becomes its maximum value and generates zero on time (t_1). Then V_{out} decreases and the minimum can be $V_{out} = V_{in}$ in a Boost Converter. Going down towards V_{in}, the output V_{out} automatically enters the previous two modes (i.e. follower boost mode or constant output voltage mode) and hence output voltage V_{out} cannot reach input voltage V_{in} as long as the PFC Controller provides a duty ratio for the operation of the boost-converter.

Sensing of Inductor Current and Input Voltage

The PFC Controller senses the inductor current I_L by the current sense circuit scheme of Figure-16a. The device maintains the voltage at CS point to be zero voltage i.e. $V_S \approx 0$ so that equation (25) i.e. $I_S = \frac{R_{CS}}{R_S} I_L$ gets formulated. This scheme has advantage of the minimum number of components for current sensing and the inrush current limitation by the resistor R_{CS}. Hence the sense current I_S represents the inductor current I_L and is used in PFC duty modulation to generate multiplier voltage V_M.

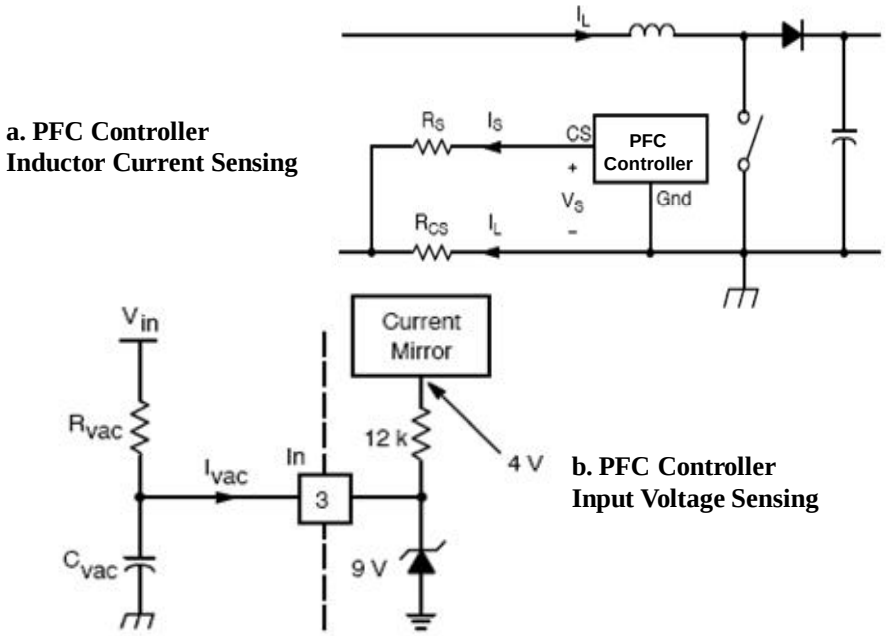


Figure-16: Inductor Current and Input Voltage Sensing by PFC Controller

The PFC Controller senses the RMS input voltage V_{ac} by the sensing scheme in Figure-16b. The internal current mirror is with a typical 4V offset voltage at its input so that the current I_{Vac} can be derived as we noted earlier (24) i.e. $I_{Vac} = \frac{\sqrt{2}V_{ac} - 4V}{R_{Vac} + 12k\Omega} \approx \frac{V_{ac}}{R'_{Vac}}$. An external capacitor V_{ac} is to maintain the In-point voltage in the calculations to always be the peak of the sinusoidal voltage due to little current consumption i.e. $V_{in} = \sqrt{2}V_{ac}$ and $I_{Vac} \approx 0$. This I_{Vac} current represents the RMS input voltage V_{ac} and is used in the PFC duty modulation.

There is an internal 9V ESD Zener Diode on the I_{in} point of the PFC Controller as shown in Figure-16b. Hence the value of R_{Vac} is at least $938k\Omega$ for 400V instantaneous input voltage surge.

$$\frac{R_{Vac}}{400V - 9V} > \frac{12k\Omega}{9V - 4V}; \qquad R_{Vac} > 938k\Omega \qquad (33)$$

Both the sensing circuit is given in Figure-17a, for boost converter control by PFC Controller. This Boost Converter output DC Voltage (390V) is used for second stage converter which is a Buck-Converter with Current Mode PWM controls. The Boost Converter PFC operates at 100 KHz and the second stage Power Converter Operates at 80 KHz switching frequency. The Figure-17b gives the total configuration of the ECPS SM 100 AC-DC model, for final output 5V, 15V, 24V.

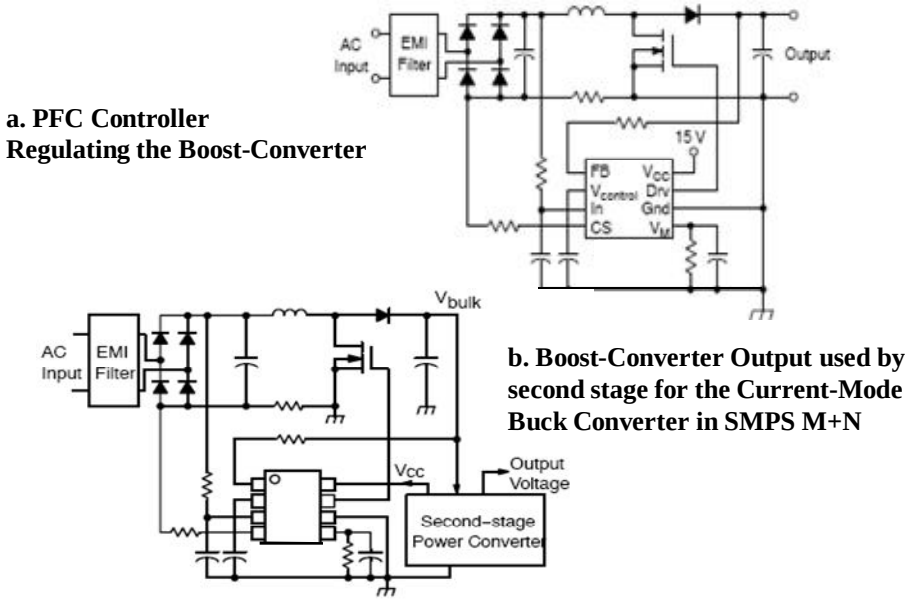


Figure-17: The Boost Converter Full Schematic

The Power Quality Testing Results

The power quality tests are carried out in EMI/EMC Center of ECIL, with Power Quality Test Equipment-AMETEK US make. This equipment has Variable 115V-300V 16Hz-1000Hz source and also variable DC 115V-300V source of 15KVA rating. This is used to power the equipment under test, and record the parameters. Figure-18 depicts the Test-set up where ECPS system is connected to this source. The Tests were carried out for single ECPS, Multiple ECPS, and ECPS sharing loads equally in current share mode. The computer records the data and generates the report about the test-is given in Figure-19. Figure-20 shows the current and voltage waveform of ECPS without PFC Circuitry with full load. Figure-21 gives the Harmonic Contents for the ECPS without PFC Circuitry; these are early embodiments used. The Table-2 gives the Current Test Result Summary for the ECPS 100W without PFC Circuitry.

From the Table-2, we get $I_{peak} = 5.787\text{A}$ and RMS value of the current wave as $I_{RMS} = 1.248\text{A}$ thus we get Crest Factor as $\text{CF} = 5.787/1.248 = 4.63$. From sinusoidal part i.e. the RMS value of fundamental current i.e. 0.529A and Power Reading i.e. 126W. From these we obtain the Displacement Power Factor (pf_{disp}) as $\text{pf}_{\text{disp}} = 126.8\text{W}/(240.40\text{V} \times 0.529\text{A}) = 0.997$. Here the displacement power factor is coming close to unity. We write from above Table-2, for I-THD as 216.50%, gives us $\text{THD}_{\text{I}} = 216.50\%$. From this distortion (or harmonic) power factor we obtain as $\text{pf}_{\text{dist}} = 1/\sqrt{1+(\text{THD}_{\text{I}}/100)^2} = 1/\sqrt{1+(216.5/100)^2} = 0.42$. Thus we get the true power factor as $\text{pf}_{\text{true}} = \text{pf}_{\text{disp}} \times \text{pf}_{\text{dist}} = 0.4187$; a very low value without PFC Circuitry.

Figure-18: The Power Quality Testing Equipment Connected to ECPS (left showing testing of single ECPS unit, right showing the testing of Multiple ECPS units)

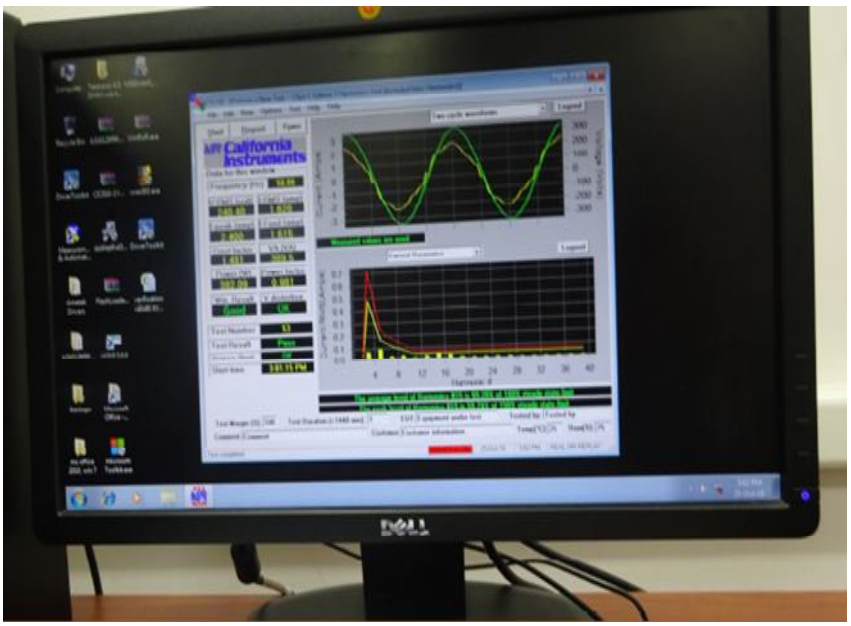


Figure-19: The computer record of data for input voltage and input current wave-form and display of harmonic contents of input current

Harmonics – Class-C per Ed. 3.2 (2009)(Run time) incl. inter-harmonics

EUT: Equipment under test — Tested by: Tested by
Test category: Class-C per Ed. 3.2 (2009) (European limits) — Test Margin: 100
Test date: 26-Oct-16 — Start time: 2:19:09 PM — End time: 2:20:31 PM
Test duration (min): 1 — Data file name: H-000058.cts_data
Comment: Comment
Customer: Customer information

Test Result: Fail — Source qualification: Normal

Current & voltage waveforms

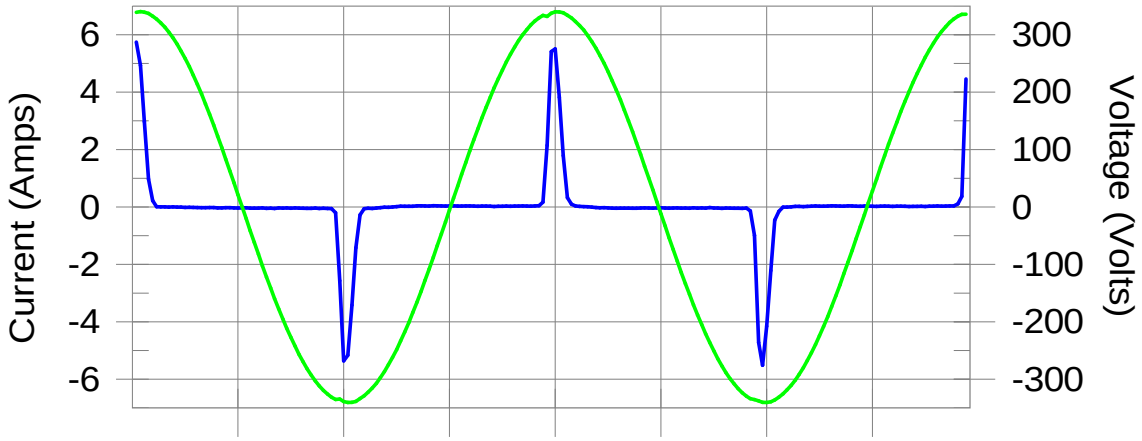
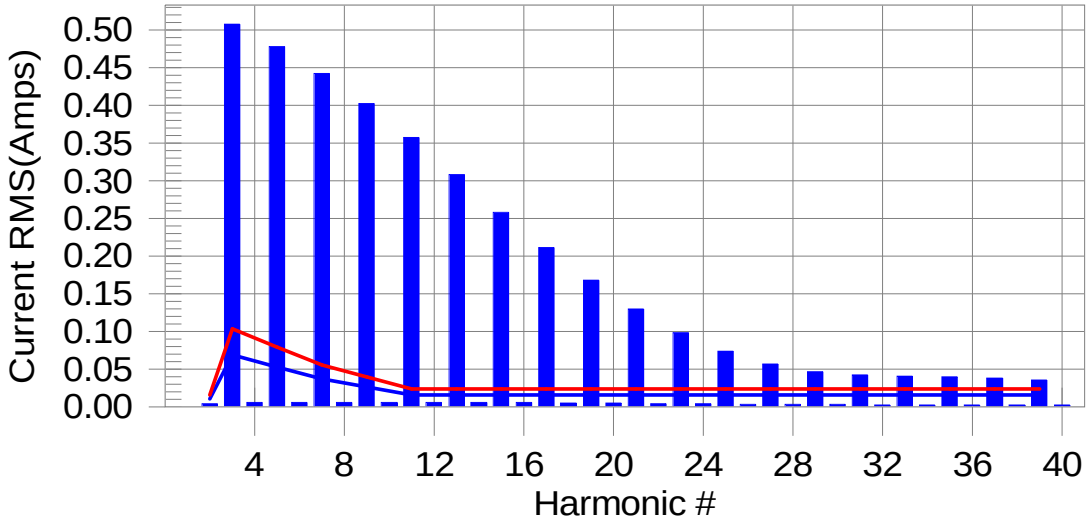


Figure-20: Current Voltage Waveform for ECPS 100W 5V with out PFC Circuitry



Test result: Fail Worst harmonics H11-2255.59% of 100% limit, H11-1522.66% of 150% limit.

Figure-21: Harmonic Contents for ECPS 100W 5V with out PFC Circuitry

Current Test Result Summary (Run time)

EUT: Equipment under test — Tested by: Tested by
Test category: Class-C per Ed. 3.2 (2009) (European limits) — Test Margin: 100
Test date: 26-Oct-16 — Start time: 2:19:09 PM — End time: 2:20:31 PM
Test duration (min): 1 — Data file name: H-000058.cts_data
Comment: Comment
Customer: Customer information

Test Result: Fail — Source qualification: Normal

THC(A): 1.12 — I-THD(%): 216.50 — POHC(A): 0.214 — POHC Limit(A): 0.050

Highest parameter values during test:

V_RMS (Volts):	240.40	Frequency(Hz):	50.00
I_Peak (Amps):	5.787	I_RMS (Amps):	1.248
I_Fund (Amps):	0.529	Crest Factor:	4.645
Power (Watts):	126.8	Power Factor:	0.436

Harm#	Harms(avg)	100%Limit	%of Limit	Harms(max)	150%Limit	%of Limit	Status
2	0.005	0.011	44.3	0.005	0.016	0.00	Pass
3	0.508	0.069	735.5	0.508	0.104	490.81	Fail
4	0.007						
5	0.478	0.053	904.6	0.479	0.079	604.48	Fail
6	0.007						
7	0.443	0.037	1196.3	0.445	0.055	801.39	Fail
8	0.007						
9	0.403	0.026	1525.1	0.406	0.040	1025.12	Fail
10	0.007						
11	0.358	0.016	2255.6	0.362	0.024	1522.66	Fail
12	0.007						
13	0.308	0.016	1944.9	0.314	0.024	1320.10	Fail
14	0.007						
15	0.259	0.016	1633.5	0.265	0.024	1115.92	Fail
16	0.007						
17	0.212	0.016	1337.6	0.219	0.024	920.74	Fail
18	0.006						
19	0.169	0.016	1064.7	0.176	0.024	739.02	Fail
20	0.006						
21	0.131	0.016	823.3	0.137	0.024	576.40	Fail
22	0.006						
23	0.099	0.016	623.3	0.104	0.024	439.17	Fail
24	0.005						
25	0.074	0.016	469.6	0.079	0.024	330.69	Fail
26	0.005						
27	0.057	0.016	362.6	0.060	0.024	252.13	Fail
28	0.004						
29	0.048	0.016	300.2	0.048	0.024	203.29	Fail
30	0.004						
31	0.043	0.016	271.9	0.045	0.024	187.16	Fail
32	0.004						
33	0.041	0.016	260.9	0.043	0.024	181.71	Fail
34	0.003						
35	0.040	0.016	253.6	0.042	0.024	175.50	Fail
36	0.003						
37	0.038	0.016	242.7	0.039	0.024	165.22	Fail
38	0.003						
39	0.036	0.016	224.9	0.036	0.024	151.19	Fail
40	0.003						

Table-2: Current Test Result Summary for ECPS 100W without PFC Circuitry

Figure-22 and 23 are for ECPS 100W 5V with PFC Circuitry on full load

Harmonics – Class-C per Ed. 3.2 (2009)(Run time) incl. inter-harmonics

EUT: Equipment under test **Tested by: Tested by**
Test category: Class-C per Ed. 3.2 (2009) (European limits) **Test Margin: 100**
Test date: 25-Oct-16 **Start time: 2:29:34 PM** **End time: 2:30:55 PM**
Test duration (min): 1 **Data file name: H-000049.cts_data**
Comment: Comment
Customer: Customer information

Test Result: Pass **Source qualification: Normal**

Current & voltage waveforms

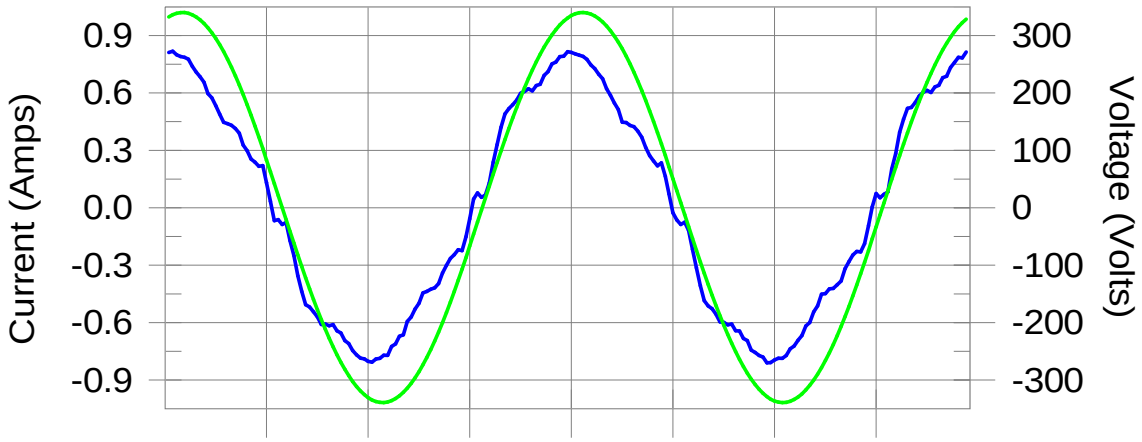
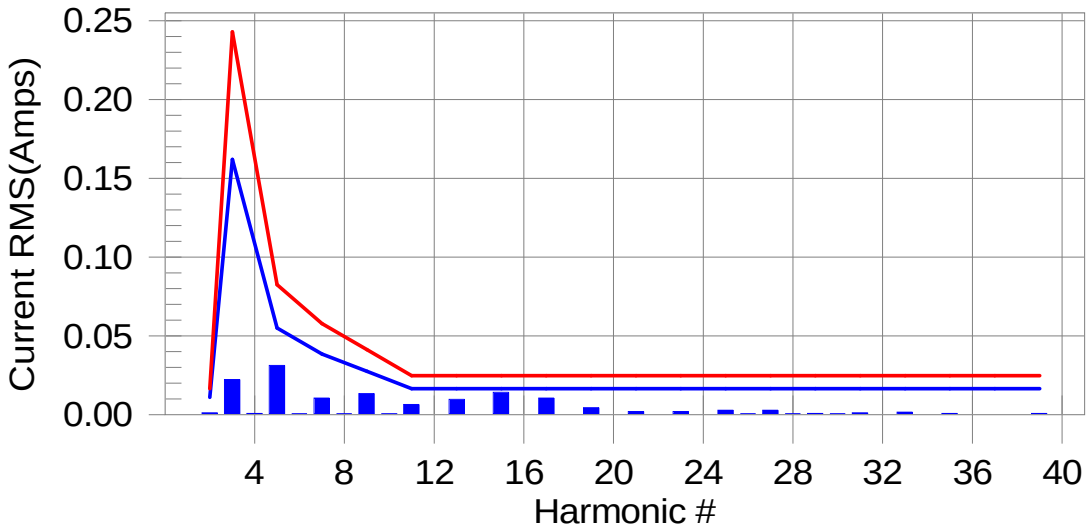


Figure-22: Current Voltage Waveform for ECPS 100W 5V with PFC Circuitry



Test result: Pass Worst harmonics H15-86.66% of 100% limit, H15-58.04% of 150% limit.

Figure-23: Harmonic Contents for ECPS 100W 5V with PFC Circuitry

Current Test Result Summary (Run time)

EUT: Equipment under test — Tested by: Tested by
Test category: Class-C per Ed. 3.2 (2009) (European limits) — Test Margin: 100
Test date: 25-Oct-16 — Start time: 2:29:34 PM — End time: 2:30:55 PM
Test duration (min): 1 — Data file name: H-000049.cts_data
Comment: Comment
Customer: Customer information

Test Result: Pass — Source qualification: Normal

THC(A): 0.05 — I-THD(%): 8.79 — POHC(A): 0.000 — POHC Limit(A): 0.052

Highest parameter values during test:

V_RMS (Volts):	240.43	Frequency(Hz):	50.00
I_Peak (Amps):	0.833	I_RMS (Amps):	0.553
I_Fund (Amps):	0.550	Crest Factor:	1.509
Power (Watts):	130.2	Power Factor:	0.981

Harm#	Harms(avg)	100%Limit	%of Limit	Harms(max)	150%Limit	%of Limit	Status
2	0.001	0.011	11.7	0.002	0.017	0.00	Pass
3	0.022	0.162	13.8	0.023	0.243	9.36	Pass
4	0.001						
5	0.031	0.055	56.8	0.031	0.083	37.97	Pass
6	0.001						
7	0.011	0.039	27.6	0.011	0.058	18.59	Pass
8	0.000						
9	0.014	0.028	49.4	0.014	0.041	33.30	Pass
10	0.000						
11	0.007	0.017	40.0	0.007	0.025	27.43	Pass
12	0.000						
13	0.010	0.017	60.3	0.010	0.025	40.47	Pass
14	0.000						
15	0.014	0.017	86.7	0.014	0.025	58.04	Pass
16	0.000						
17	0.011	0.017	64.9	0.011	0.025	43.43	Pass
18	0.000						
19	0.005	0.017	27.5	0.005	0.025	0.00	Pass
20	0.000						
21	0.002	0.017	12.2	0.002	0.025	0.00	Pass
22	0.000						
23	0.002	0.017	12.4	0.002	0.025	0.00	Pass
24	0.000						
25	0.003	0.017	18.4	0.004	0.025	0.00	Pass
26	0.000						
27	0.003	0.017	16.9	0.003	0.025	0.00	Pass
28	0.000						
29	0.001	0.017	5.8	0.001	0.025	0.00	Pass
30	0.000						
31	0.001	0.017	8.9	0.002	0.025	0.00	Pass
32	0.000						
33	0.002	0.017	10.2	0.002	0.025	0.00	Pass
34	0.000						
35	0.001	0.017	5.7	0.001	0.025	0.00	Pass
36	0.000						
37	0.000	0.017	1.9	0.000	0.025	0.00	Pass
38	0.000						
39	0.001	0.017	5.3	0.001	0.025	0.00	Pass
40	0.000						

Table-3: Current Test Result Summary for ECPS 100W with PFC Circuitry

From the Table-3, we get $I_{peak} = 0.833A$ and RMS value of the current wave as $I_{RMS} = 0.553A$ thus we get Crest Factor as $CF = 0.833/0.553 = 1.5051$. From sinusoidal part i.e. the RMS value of fundamental current i.e. 0.550A and Power Reading i.e. 130.2W. From these we obtain the Displacement Power Factor (pf_{disp}) as $pf_{disp} = 130.2W/(240.43V \times 0.550A) = 0.9845$. Here the displacement power factor is coming close to unity. We write from above Table-3, for I-THD as 8.79%, gives us $THD_I = 8.79\%$. From this distortion (or harmonic) power factor we obtain as $pf_{dist} = 1/\sqrt{1+(THD_I/100)^2} = 1/\sqrt{1+(8.79/100)^2} = 0.9962$. Thus we get the true power factor as $pf_{true} = pf_{disp} \times pf_{dist} = 0.981$; a good value with PFC Circuitry

The comparison of circuit of ECPS 100W at full load, with and without PFC circuit indicates the improvement in the quality of power drawn from AC mains. Not only is the true power factor improved, but also the total harmonic distortion and the crest factor. The ECPS with PFC Circuitry results show the test passed as per IEC-61000-3-2 power quality standards. In short we find current drawn from AC Mains is almost sinusoidal and almost with phase of the input voltage, when the active PFC circuit is used.

Harmonics – Class-C per Ed. 3.2 (2009)(Run time) incl. inter-harmonics

EUT: Equipment under test **Tested by: Tested by**
Test category: Class-C per Ed. 3.2 (2009) (European limits) **Test Margin: 100**
Test date: 25-Oct-16 **Start time: 3:01:15 PM** **End time: 3:02:37 PM**
Test duration (min): 1 **Data file name: H-000053.cts_data**
Comment: Comment
Customer: Customer information

Test Result: Pass **Source qualification: Normal**

Current & voltage waveforms

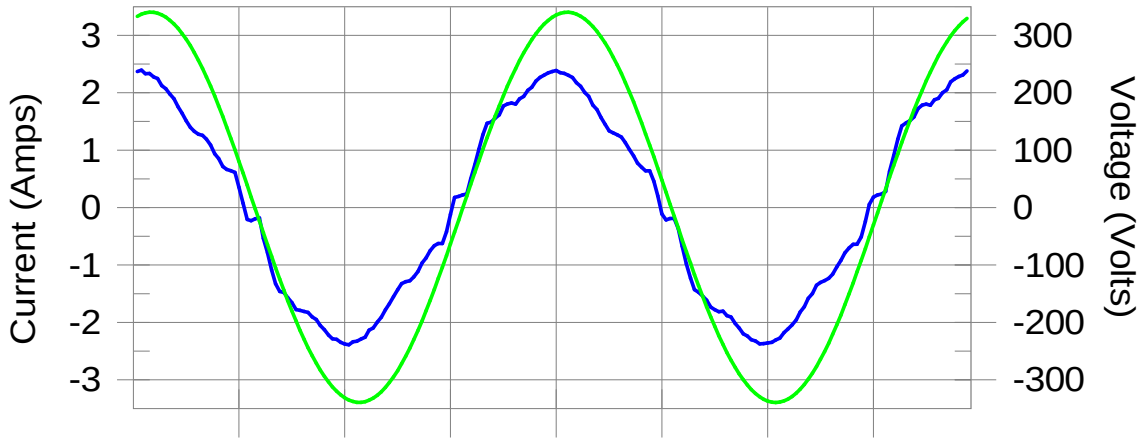
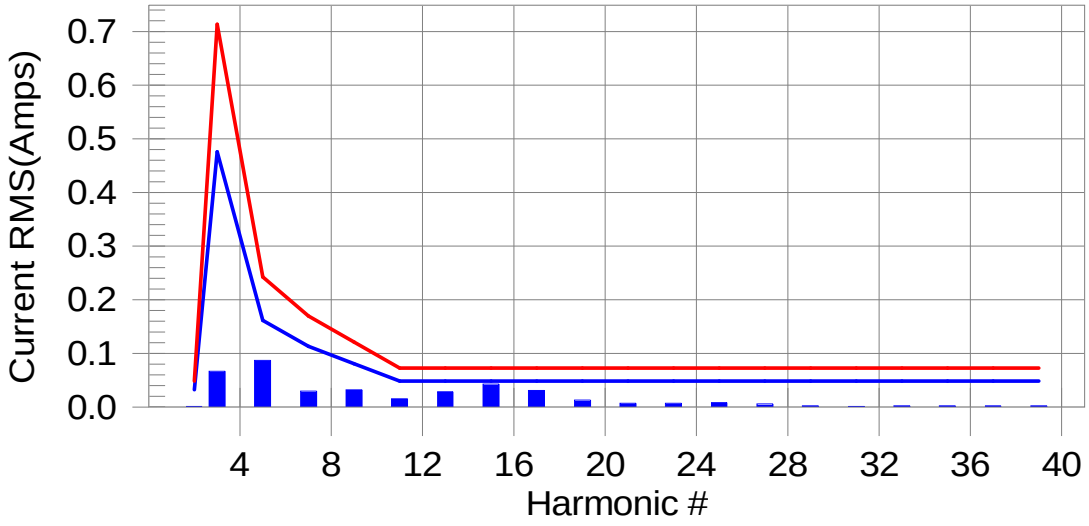


Figure-24: Current and Voltage Waveforms for 5V, 15V, 24V ECPS100 together on full load with PFC Circuitry

Harmonics and Class C limit line European Limits



Test result: Pass Worst harmonics H15-89.20% of 100% limit, H15-59.74% of 150% limit.

Figure-25: Harmonic Contents for ECPS 100W 5V, 15V, 24V together fully loaded with PFC Circuitry

Current Test Result Summary (Run time)

EUT: Equipment under test Tested by: Tested by
Test category: Class-C per Ed. 3.2 (2009) (European limits) Test Margin: 100
Test date: 25-Oct-16 Start time: 3:01:15 PM End time: 3:02:37 PM
Test duration (min): 1 Data file name: H-000053.cts_data
Comment: Comment
Customer: Customer information

Test Result: Pass Source qualification: Normal

THC(A): 0.14 I-THD(%): 8.54 POHC(A): 0.000 POHC Limit(A): 0.153

Highest parameter values during test:

V_RMS (Volts):	240.41	Frequency(Hz):	50.00
I_Peak (Amps):	2.417	I_RMS (Amps):	1.624
I_Fund (Amps):	1.617	Crest Factor:	1.491
Power (Watts):	382.5	Power Factor:	0.981

Table-4: Current Test Result Summary for ECPS 100W with PFC Circuitry: 5V, 15V, 24V together full loaded

Harmonics – Class-C per Ed. 3.2 (2009)(Run time) incl. inter-harmonics

EUT: Equipment under test — Tested by: Tested by
Test category: Class-C per Ed. 3.2 (2009) (European limits) — Test Margin: 100
Test date: 26-Oct-16 — Start time: 11:56:53 AM — End time: 11:58:14 AM
Test duration (min): 1 — Data file name: H-000057.cts_data
Comment: Comment
Customer: Customer information

Test Result: Pass — Source qualification: Normal

Current & voltage waveforms

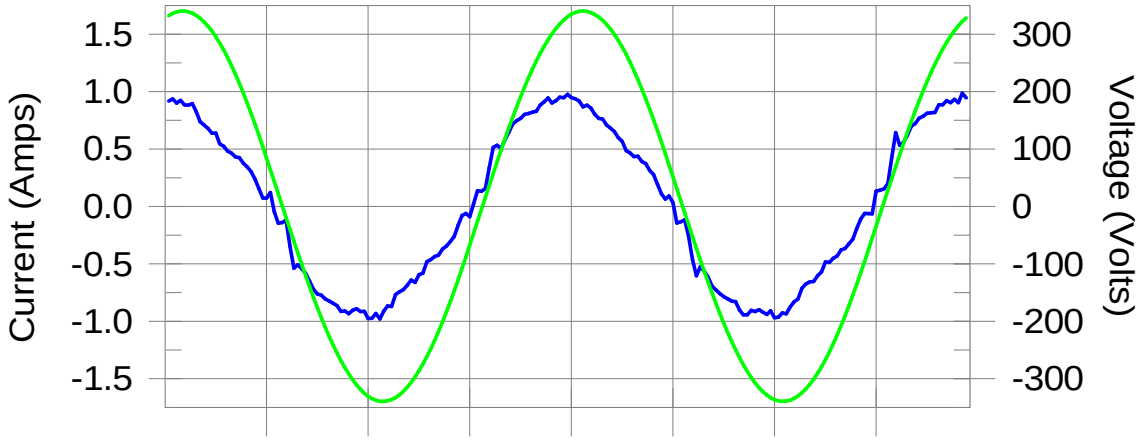
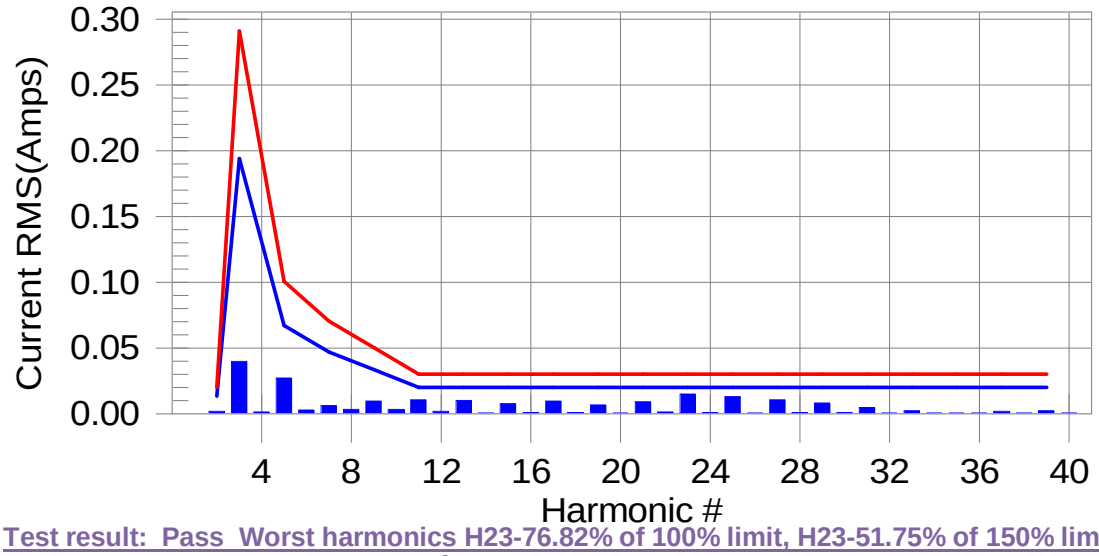


Figure-26: Current and Voltage Waveforms for TWO-15V ECPS100 together sharing 8A load with PFC Circuitry

Harmonics and Class C limit line — European Limits



Test result: Pass Worst harmonics H23-76.82% of 100% limit, H23-51.75% of 150% limit.

Figure-27: Harmonic Contents for ECPS 100W 15V TWO together sharing 8A load with PFC Circuitry

Current Test Result Summary (Run time)

EUT: Equipment under test **Tested by: Tested by**
Test category: Class-C per Ed. 3.2 (2009) (European limits) **Test Margin: 100**
Test date: 26-Oct-16 **Start time: 11:56:53 AM** **End time: 11:58:14 AM**
Test duration (min): 1 **Data file name: H-000057.cts_data**
Comment: Comment
Customer: Customer information

Test Result: Pass **Source qualification: Normal**

THC(A): 0.06 **I-THD(%): 9.20** **POHC(A): 0.027** **POHC Limit(A): 0.064**

Highest parameter values during test:

V_RMS (Volts):	**240.42**	**Frequency(Hz):**	**50.00**
I_Peak (Amps):	**1.098**	**I_RMS (Amps):**	**0.674**
I_Fund (Amps):	**0.671**	**Crest Factor:**	**1.634**
Power (Watts):	**156.1**	**Power Factor:**	**0.963**

Table-5: Current Test Result Summary for ECPS 100W with PFC circuit 15V two of them sharing 8A load

There are nine such test reports with different configurations kept at CAD ECIL.

Product Embodiments since 1993

The first phase is called ECPS-I, where basic inherent load sharing was demonstrated. This product was well utilized in very large numbers by ECIL for NPCIL power plant control and instrumentation systems from Kaiga-1 & 2 to PHWR-500 TAPP 3 & 4; and then to Kaiga 3 & 4 and RAPP 5 & 6.

Few of these were employed in up-gradation of C&I for- Dhruva reactor, NAPP 1&2, KAPP 1&2, and MAPP 1&2. The second phase called ECPS-II had forced share daisy chain circuit to forcefully and equally share the load current, despite wide difference in individual voltage setting of each module. This circuit modification now has been retrofitted in older plants also-by doing site modification in earlier ECPS-I. Various stages of product development since 1993 at BARC and ECIL are depicted in Figure-28. Based on feedback from all users the third generation advancement of the earlier models (embodiments) was taken up in mid-2006. This new product [8], [9] is complete, (1) with two front panel displays (for unit voltage and unit current), (2) with reduction in width, (3) with inclusion of forced third wire current sharing circuit, (4) with voltage adjustment in front-panel, (5) with in built circuits to have good input Power Factor by employing active Power Factor Correction (PFC) circuitry along Total Harmonic Distortion (THD) Control-as per IEC1000-3-2 Standard. This is new-product for NPCIL PHWR-700MW reactor C&I systems. In this embodiment only 100Watt (width 16T) with two models DC-DC and AC-DC; are fabricated; for output 5V, 15V, 24V. Figure-29 show this latest embodiment.

Figure-28: Fig: 1 Few earlier embodiments of ECPS

Figure-29: Latest embodiment of ECPS SM100 fourteen of them sharing the load

Conclusions

In this note we presented the brief result of Power Quality Qualification Tests as per IEC 61000-3-2, done for a developed new product ECPS100 to be used in NPCIL-

PHWR700MW. We have qualified the equipment that is ECPS 100, with implemented active PFC circuitry, to improve input power factor and reduce the harmonic current contents; that gives a qualified system as per latest IEC standard. This note also takes up the complex issues of the power factor and its modern treatment as active power factor correction circuit and harmonic current controls scheme. This technique is modern technique to have qualified power quality as per IEC 61000-3-2. In this note we have described the scheme of Continuous Conduction Mode CCM, which is suitable for high power applications like for ECPS. The DCM i.e. Discontinuous Conduction Mode with zero current switching for PFC circuits is also used but for lower power conversion systems like LED lighting etc. However when we started this embodiment's development only very few schemes were available in 2006; but implementing the product with the described CCM scheme we have obtained our objective that we demonstrated in several results of IEC 61000-3-2 tests.

References

(1) Shantanu Das , "*Robust Switched Mode DC Power Supplies for Safety Significant & Safety-Critical Industrial Control & Instrumentation Systems*", Electrical India .Vol. 50 No.4 Issue April 10, 2010, pp. 98-107, 2010.

(2) Shantanu Das, Md. Arifuddin "*EC-SMPS Hybrid Version for Nuclear Instrumentation & Control Systems*", BARC News Letter March 2009.

(3) Shantanu Das, B.B.Biswas, "*Proprietary Electronics for Reactor Safety & Controls*", Int. J. Nuclear Energy Science & Technology Vol. 3, No.4, 2007, pp.358-369, 2008.

(4) Shantanu Das, B B Biswas, "*Fault Tolerant Power Supplies for safety significant nuclear I&C*", Int. J. Nuclear Knowledge Management IJNKM-2008, vol.3, No.1.pp59-72, 2008.

(5) Shantanu Das, B B Biswas, "*Fault Tolerant Power Distribution* SMPS (M+N) -TRADE MARK", for Trade Mark ECPS, 2001.

(6) Shantanu Das, M B Patil, DA Roy, B Ganaraj, C K Pithawa, B B Biswas, Umesh Chandra, P Sudhakar (ECIL), "*Microcomputer boards for safety and safety critical systems for nuclear power plants and other high reliable industrial application*", BARC News letter Nov 2000.

(7) International Electro Technical Commission 2010, *International Special Committee on Radio Interference* (CISPR), http://webstore.iec.ch

(8) Brochure "*Electronics Corporation Power Supply*" ECPS SM 100, 2016, ECIL

(9) EC R&D Report 2016-National Technology Day, 11 May, 2016 (Issue on 50th Year of ECIL)

(10) Electromagnetic Compatibility (EMC) low frequency standards, "*IEC-61000-3-2-Limits for Harmonic Currents Emissions*" http://www.dsce.fee.unicamp.br/~antenor/pdffiles/IEC.pdf

(11) Bollen M. H. J, "*Understanding Power Quality Problems*"; New-York: IEEE Press ISBN 0-78083-4713-7; 2000.

(12) Shantanu Das, Ramnayan Yadav, "*Conducted and Radiated Emission Tests for Fault Tolerant Power Distribution System ECPS 100 developed for PHWR700MW C&I*", BARC News Letter Sept-Oct; 2016.

(13) W. Grady and R. Gilleskie, "*Harmonics And How They Relate To Power Factor*," Proc. of the EPRI Power Quality Issues & Opportunities Conference (PQA'93), San Diego, CA 1993.